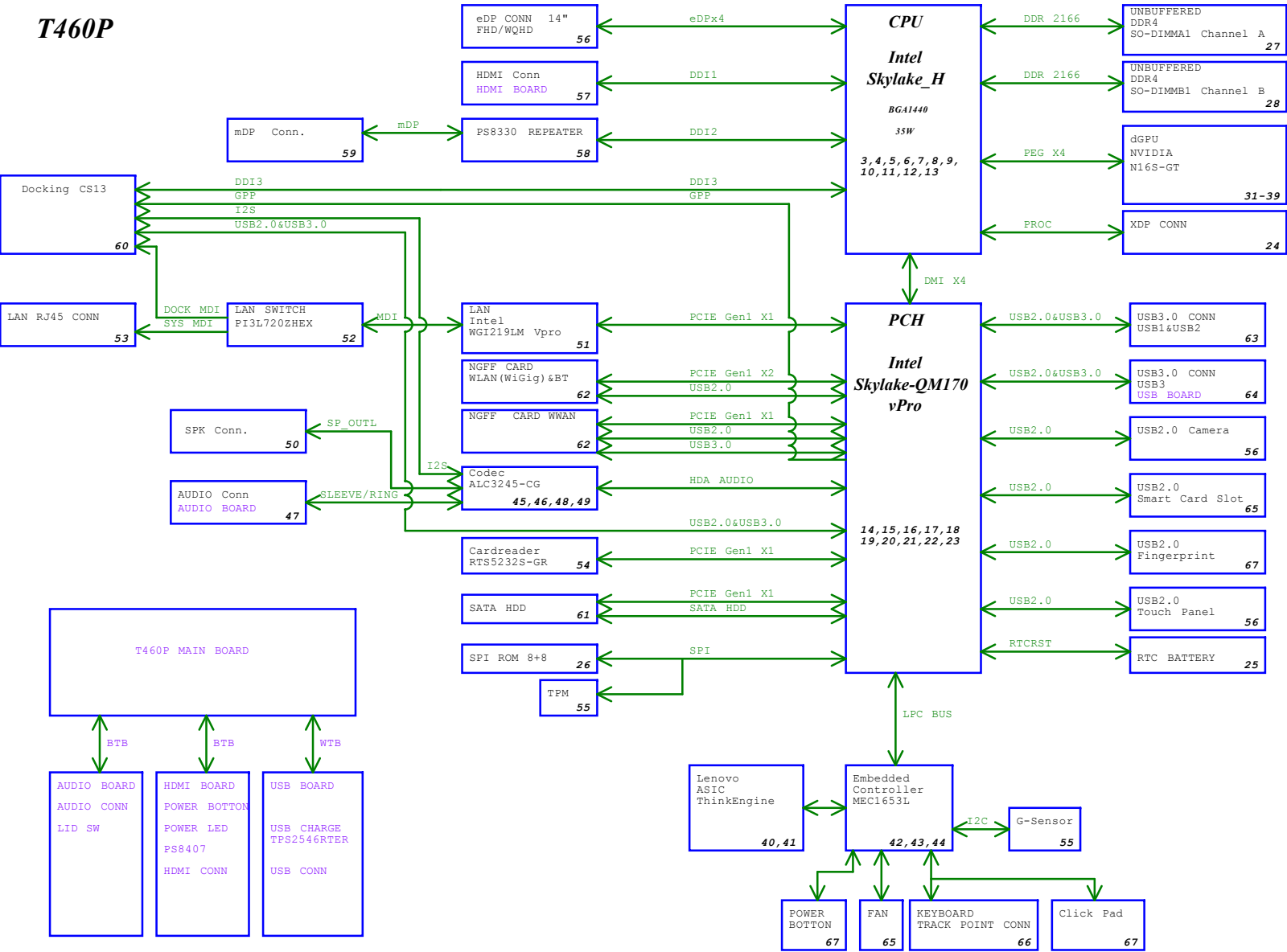


T460P



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Page:14~23==>PCH SKL-H
Page:24==>XDP CONNECTOR
Page:25==>RTC BATTERY
Page:26==>SPI FLASH
Page:27~28==>DDR4 MEMORY
Page:31~39==>N16S-GT
Page:40~41==>THINK ENGINE
Page:42~44==>MEC1653L
Page:45~50==>AUDIO ALC3245-CG
Page:51~53==>LAN WGI219LM
Page:54==>CARD READER RTS5232S-GR
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Page:72==>LOAD SW LAN
Page:73==>LOAD SW B
Page:74==>LOAD SW WWAN&WLAN
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Page:79==>SCREW HOLE
Page:80==>DC-IN
Page:81==>BATTERY INPUT
Page:82==>BATTERY CHARGER (BQ24780S)
Page:83==>DC/DC VCC5M/VCC3M
Page:84==>DC/DC IMVP8
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Page:86==>DC/DC VCCGFXCORE_I
Page:87==>DC/DC VCCSA
Page:88==>CPU PROCESSOR DECOUPLING
Page:89==>DC/DC VCCCPUIO
Page:90==>DC/DC VCC1R0 SUS
Page:91==>DC/DC VCC1R2A/VCC0R6B
Page:92==>DC/DC VCC2R5A
Page:93==>DC/DC GFXCORE_D
Page:94==>DC/DC VCC1R5VIDEO
Page:95==>DC/DC VCC1R05VIDEO_PLL

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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF	Hibernation or Shutdown	Soft Off
	S5	M3	ON	ON	ON	ON	OFF	OFF		
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G3	S5 EC OFF	M-OFF	ON	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off
	---	---	OFF	OFF	OFF	OFF	OFF	OFF		

Schematics Mark Definition

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

Tolerance
Temperature Characteristics
Rated Voltage
Package Size

BT463
DA80000Z600K4W4G1646E-BC1A
X7608112001MT41J256M16HA-093G
X7608112002H5TC4G63CFR-N0C
X7608112003

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NP0	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	+50, -20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Sensor (LIS3DH)	0011 000Xb
G-Sensor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device	Address
CH-A DDR DIMM1	1001 0000b
CH-B DDR DIMM2	1001 0010b

PCH SM Bus0 address

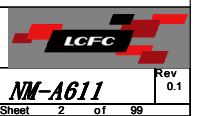
Device	Address
Intel Lan_I219	0XC8

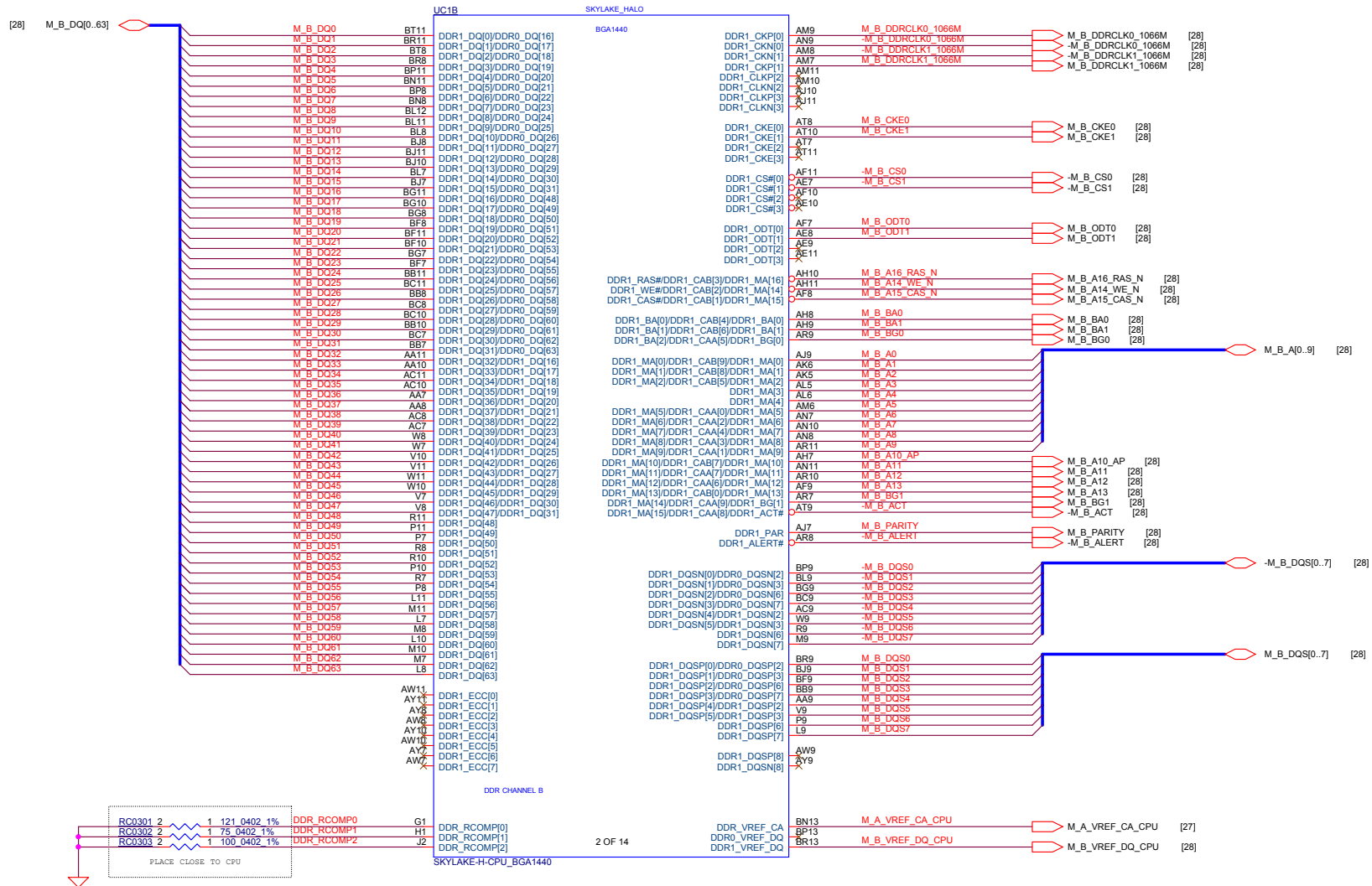
BOM Structure Table


BOM Structure	NOTE
DEBUG@	For EE DEBUG
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
GC6@	For GC6 function
NGC6@	NON GC6 function
ME@	ME Connector
EMC@	For EMI Solution
RF@	For RF Solution
VSE2G@	For SAMSUNG VRAM Setting
VME2G@	For Micron VRAM Setting
VHC2G@	For RF HYNIX VRAM Setting
X76_VSE2G@	K4W4G1646E-BC1A x4 + 24.9K
X76_VME2G@	MT41J256M16HA-093G x4 +10k
X76_VHC2G@	H5TC4G63CFR-N0C x4 +30.1k
CS@	For CURRENT SENSE
UMA@	For UMA
DIS@	For DIS
UC1@	For CPU



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						0.1	
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[31] PEG_RXP[3:0] 
[31] PEG_RXN[3:0] 

 PEG_TXP[3:0] [31]
 PEG_TXN[3:0] [31]

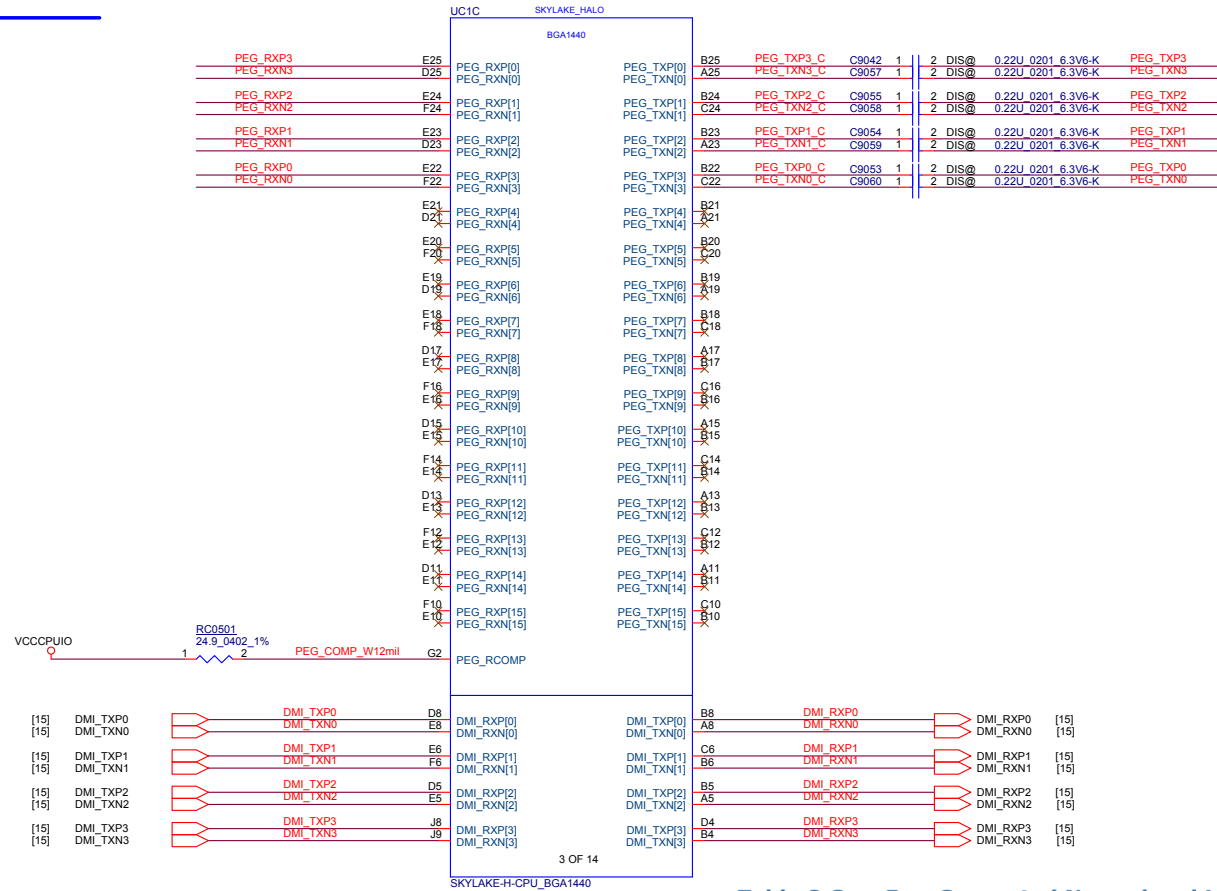



Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.For example:
 - When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

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HDMI PORT

[57] HDMI_DDIP1_2P
[57] HDMI_DDIP1_2N
[57] HDMI_DDIP1_1P
[57] HDMI_DDIP1_1N
[57] HDMI_DDIP1_0P
[57] HDMI_DDIP1_0N
[57] HDMI_DDIP1_CLK_DP
[57] HDMI_DDIP1_CLK_DN

HDMI_DDIP1_2P
HDMI_DDIP1_2N
HDMI_DDIP1_1P
HDMI_DDIP1_1N
HDMI_DDIP1_0P
HDMI_DDIP1_0N
HDMI_DDIP1_CLK_DP
HDMI_DDIP1_CLK_DN

K36
K37
J35
J34
H37
H36
J37
J38

UC1D

SKYLAKE_HALO

BGA1440

DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]

EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXN[2]
EDP_TXP[3]
EDP_TXN[3]

D29
E23
F28
E28
B29
A23
B28
C28

CPU_EDP_TX0+
CPU_EDP_TX0-
CPU_EDP_TX1+
CPU_EDP_TX1-
CPU_EDP_TX2+
CPU_EDP_TX2-
CPU_EDP_TX3+
CPU_EDP_TX3-

[56] CPU_EDP_TX0+
[56] CPU_EDP_TX0-
[56] CPU_EDP_TX1+
[56] CPU_EDP_TX1-
[56] CPU_EDP_TX2+
[56] CPU_EDP_TX2-
[56] CPU_EDP_TX3+
[56] CPU_EDP_TX3-

VCCCPUIO

RC0601
24.9_0402_1%

mDP PORT

[58] MDP_DDI2_P0
[58] MDP_DDI2_N0
[58] MDP_DDI2_P1
[58] MDP_DDI2_N1
[58] MDP_DDI2_P2
[58] MDP_DDI2_N2
[58] MDP_DDI2_P3
[58] MDP_DDI2_N3

MDP_DDI2_P0
MDP_DDI2_N0
MDP_DDI2_P1
MDP_DDI2_N1
MDP_DDI2_P2
MDP_DDI2_N2
MDP_DDI2_P3
MDP_DDI2_N3

H34
H33
F37
G38
F34
F35
E37
E36

DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]

EDP_DISP_UTIL

EDP_RCOMP

A33 Leave EDP_DISP_UTIL NC

D37 EDP_RCOMP_W12mil

DOCKING PORT

[58] MDP_DDIP2_AUXP
[58] MDP_DDIP2_AUXN

MDP_DDIP2_AUXP
MDP_DDIP2_AUXN

F26
E26
DDI2_AUXP
DDI2_AUXN

[60] DOCK_DDIP3_0P
[60] DOCK_DDIP3_0N
[60] DOCK_DDIP3_1P
[60] DOCK_DDIP3_1N
[60] DOCK_DDIP3_2P
[60] DOCK_DDIP3_2N
[60] DOCK_DDIP3_3P
[60] DOCK_DDIP3_3N

DOCK_DDIP3_0P
DOCK_DDIP3_0N
DOCK_DDIP3_1P
DOCK_DDIP3_1N
DOCK_DDIP3_2P
DOCK_DDIP3_2N
DOCK_DDIP3_3P
DOCK_DDIP3_3N

C34
D34
B35
B34
F33
E33
C33
B33

DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]

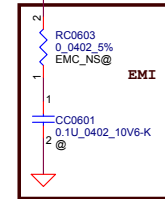
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PROC_AUDIO_SDI
PROC_AUDIO_SDO

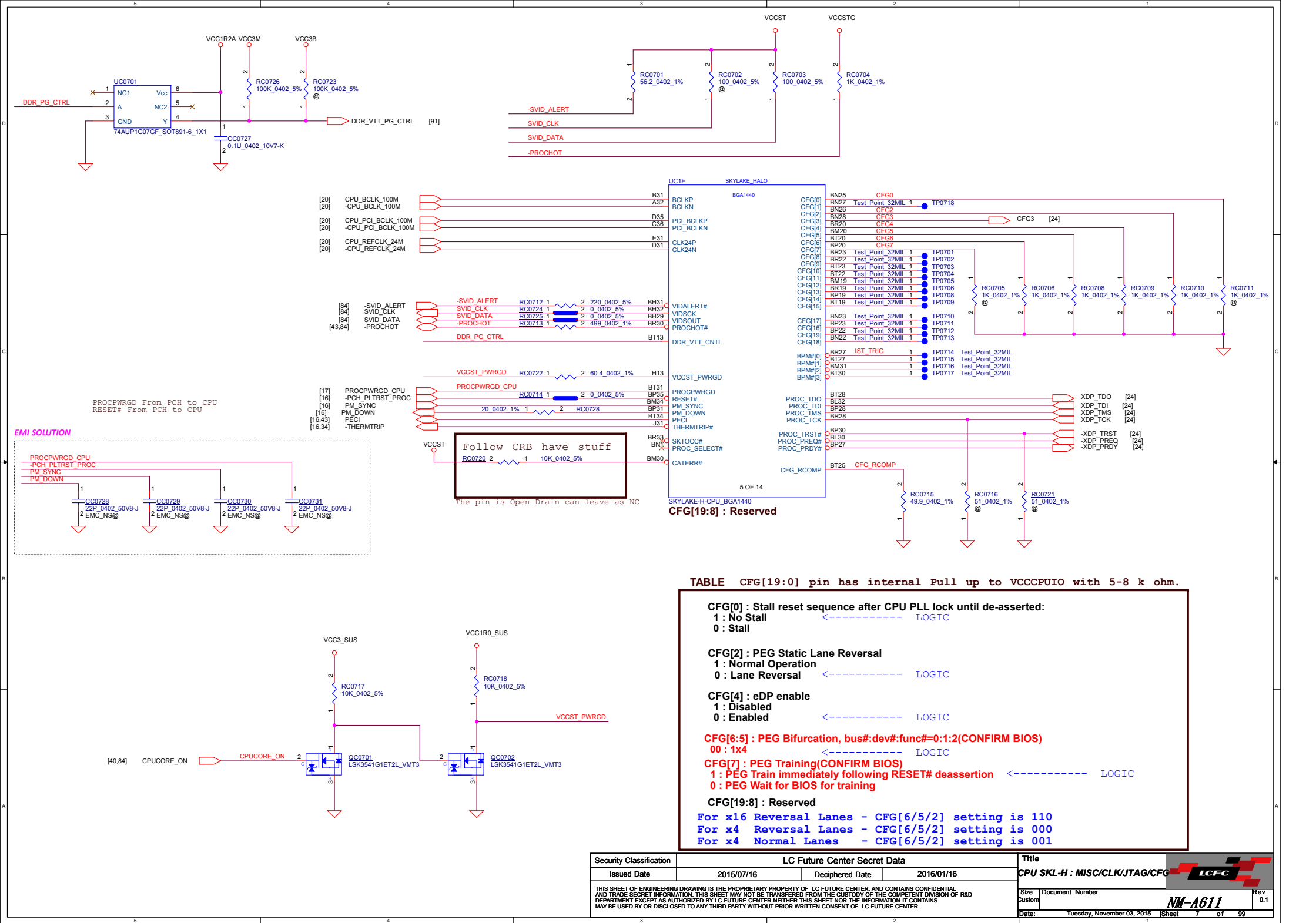
G27 PROC_AUDIO_CLK_CPU
G25 PROC_AUDIO_SDI_CPU
G29 PROC_AUDIO_SDO_CPU

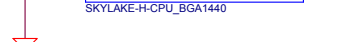
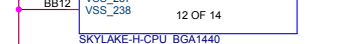
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2 RC0602


[17] PROC_AUDIO_CLK_CPU
[17] PROC_AUDIO_SDI_CPU
[17] PROC_AUDIO_SDO_CPU

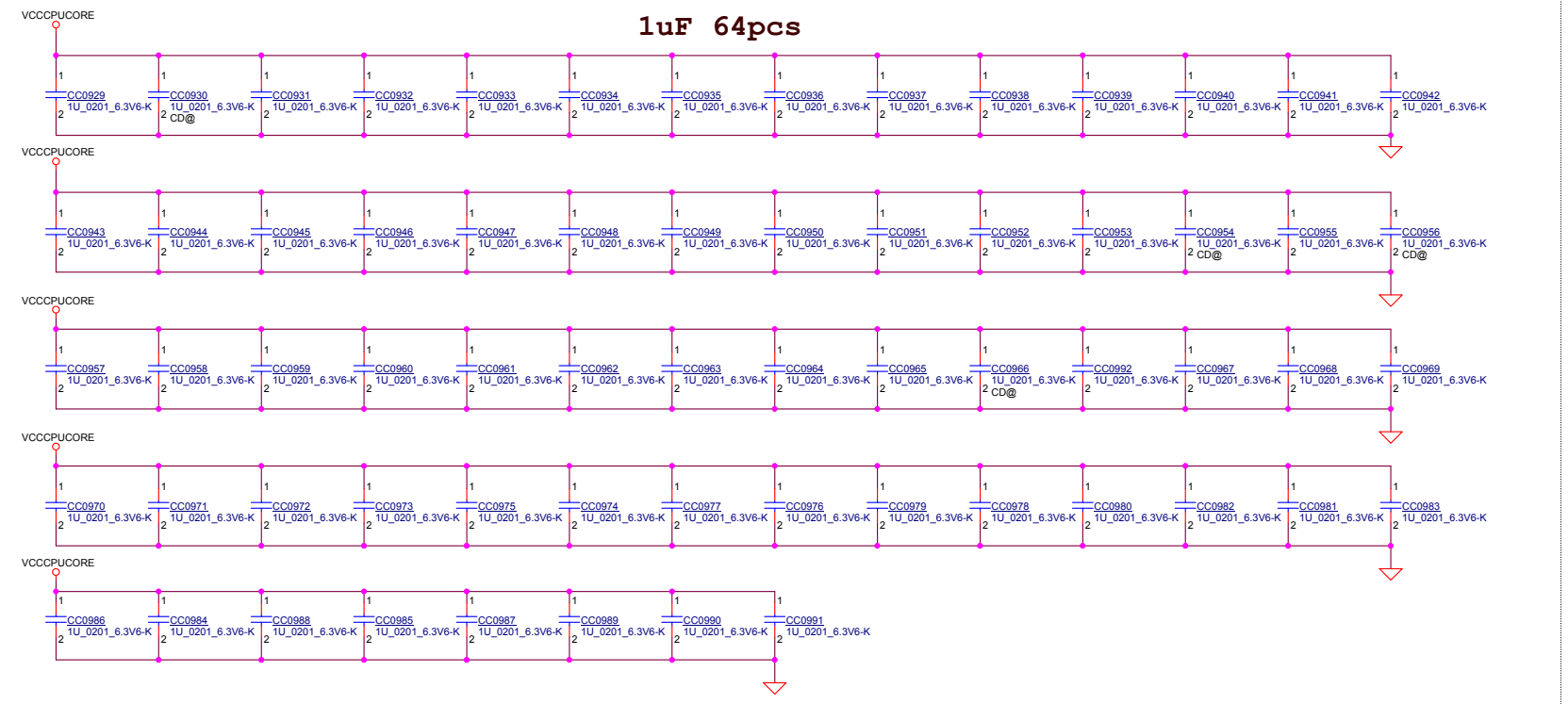
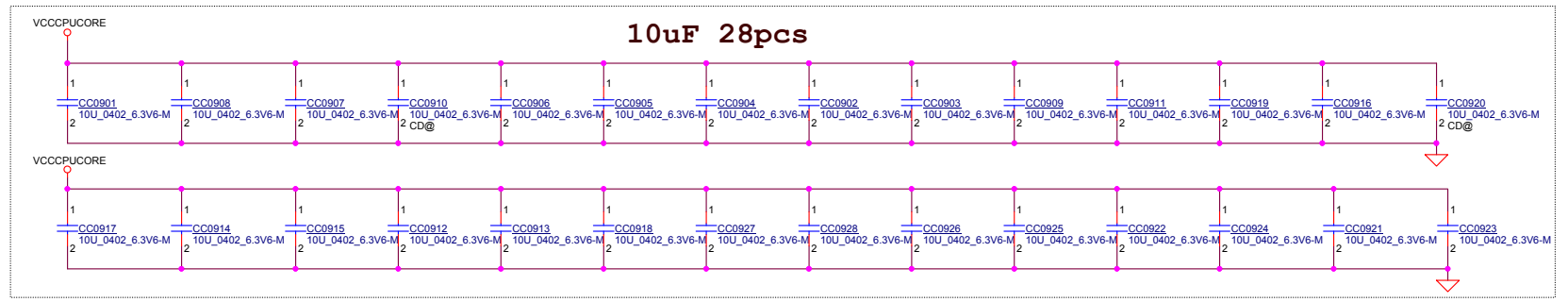
Place near CPU.



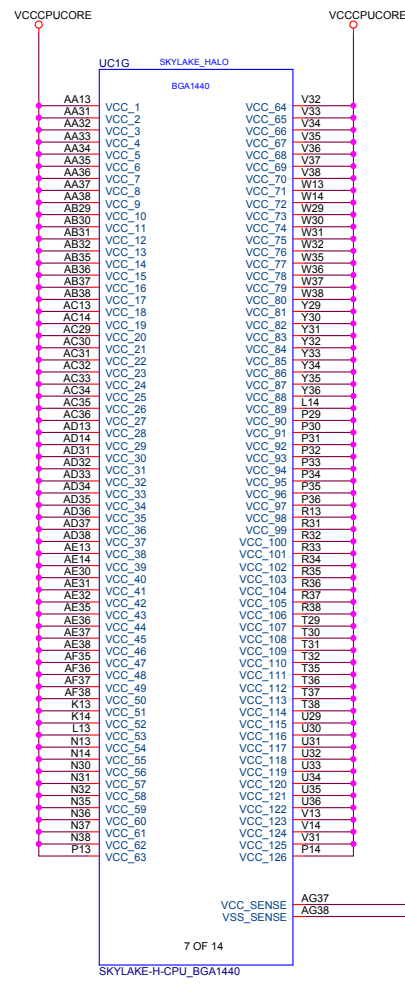
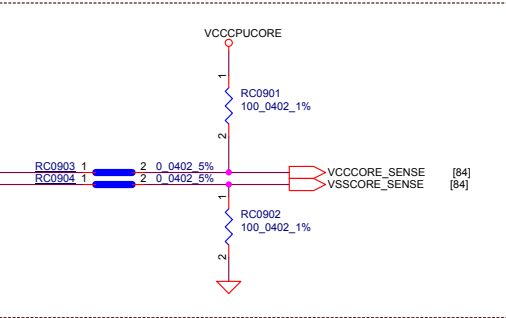




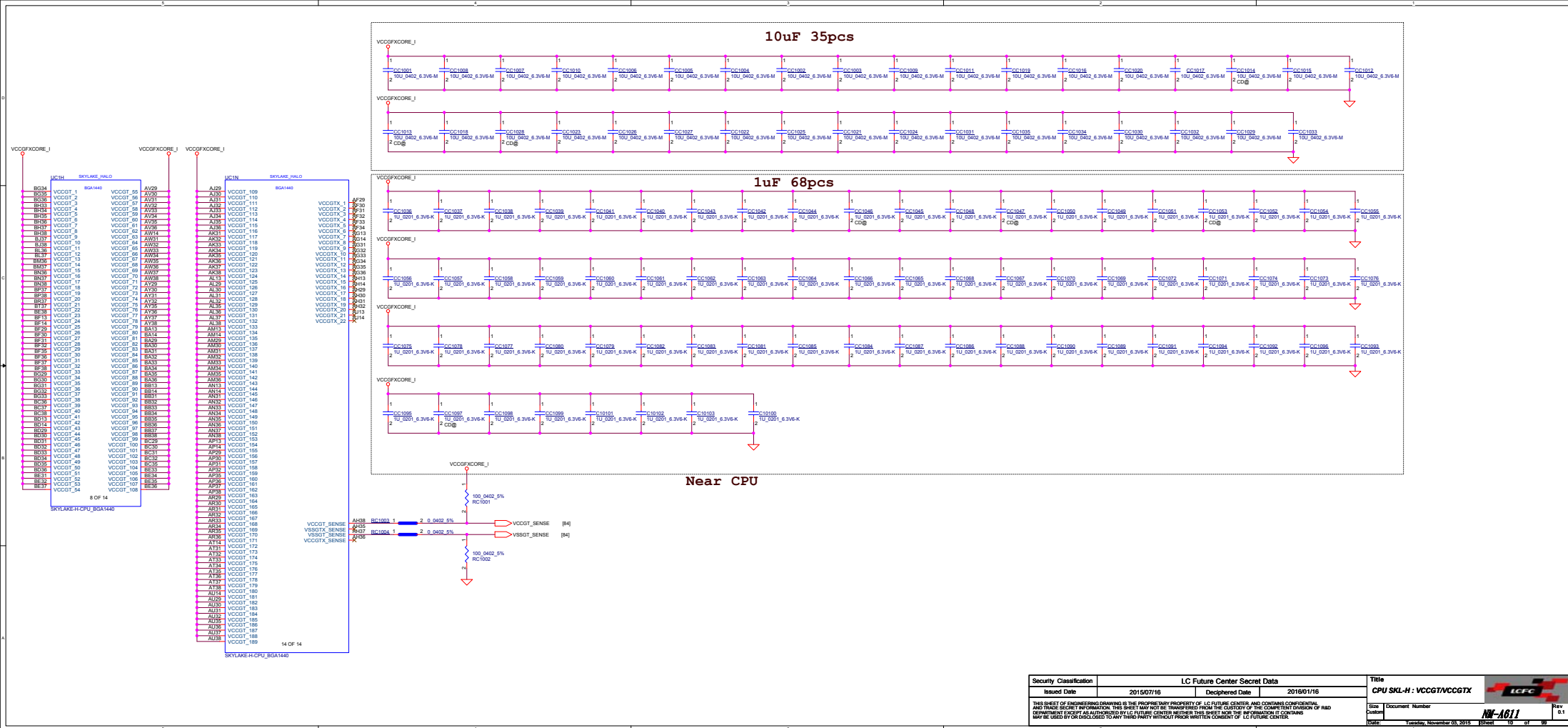
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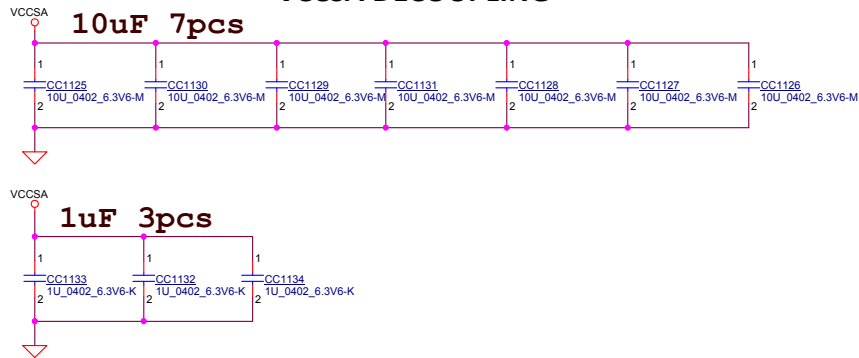
NEAR PROCESSOR PINS



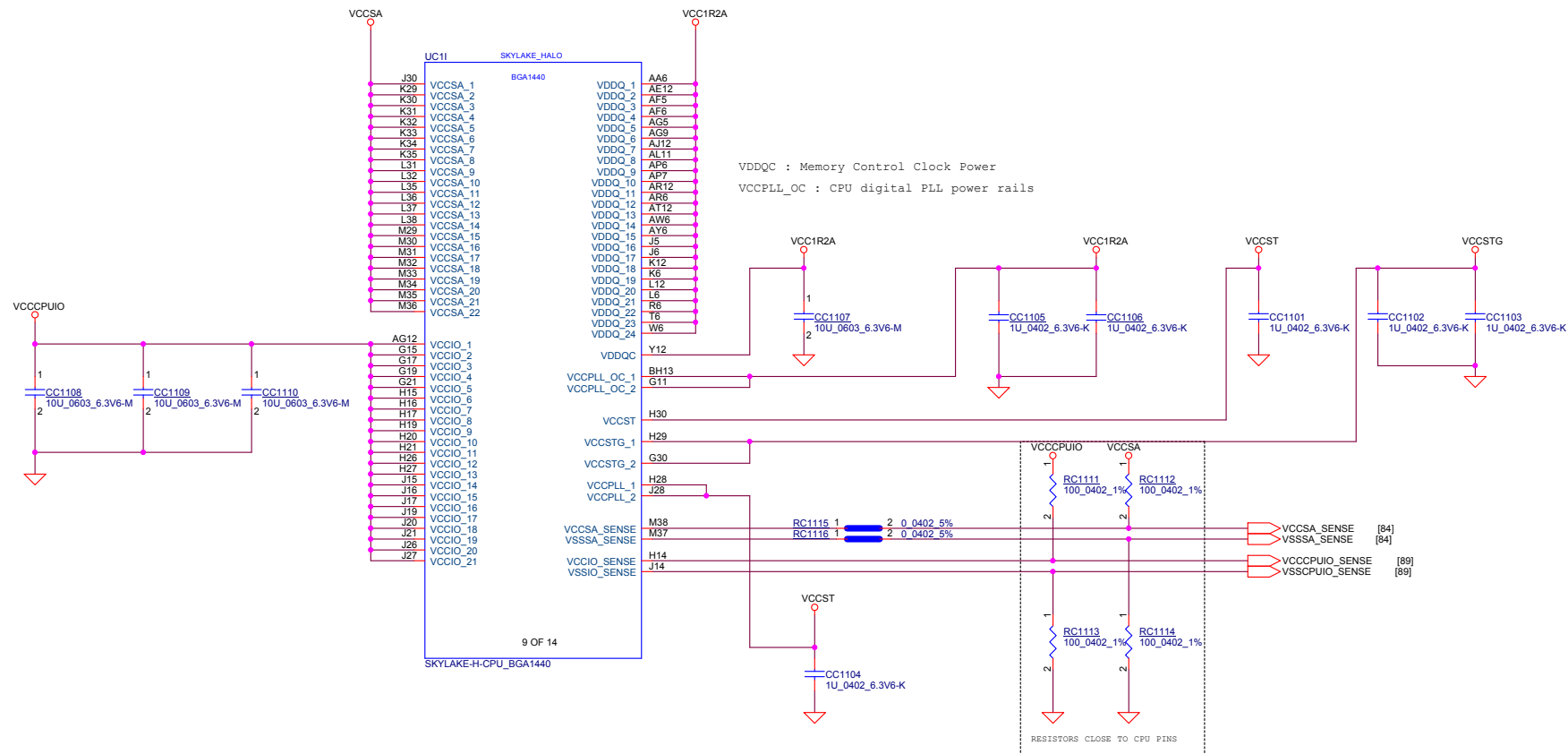
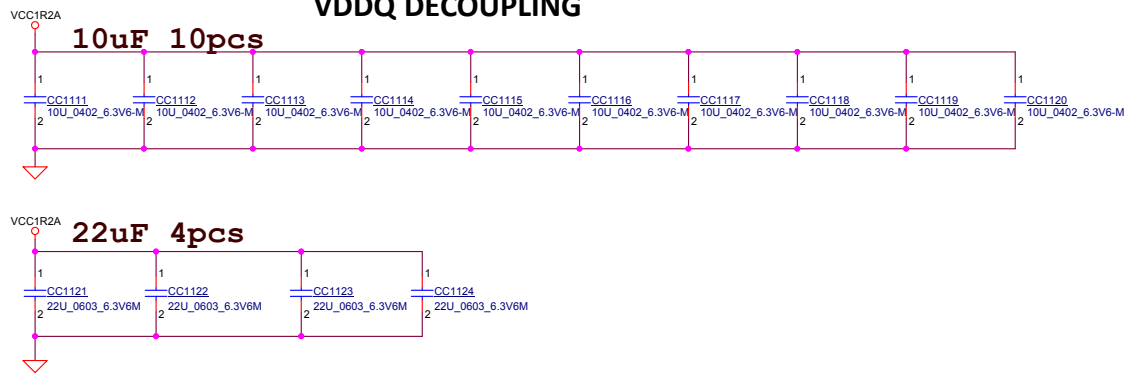
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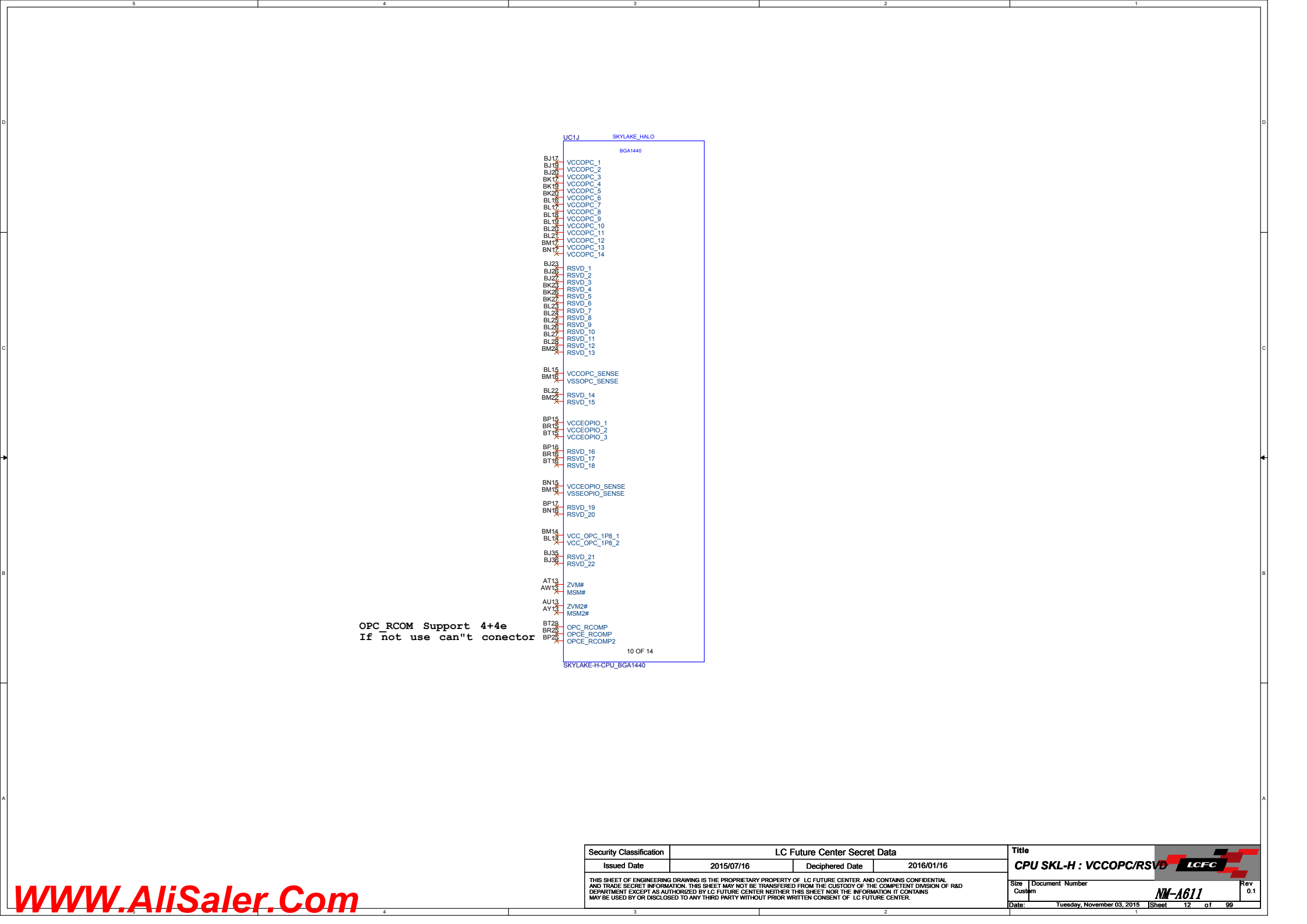


VCCSA DECOUPLING

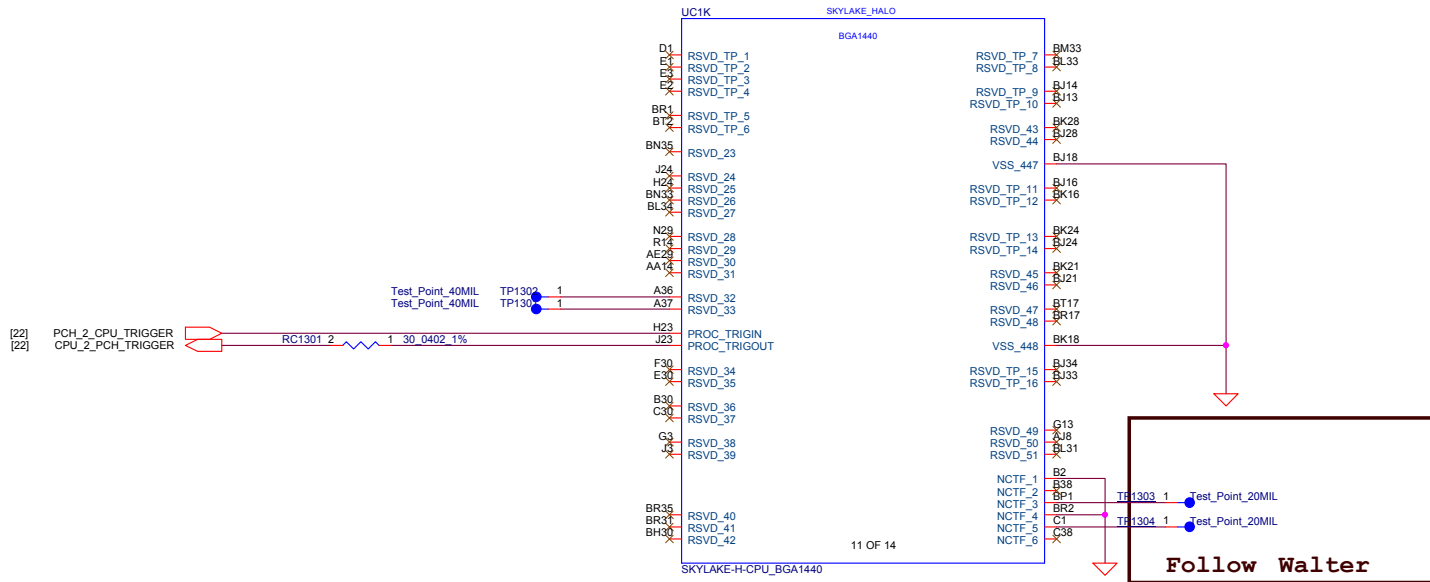


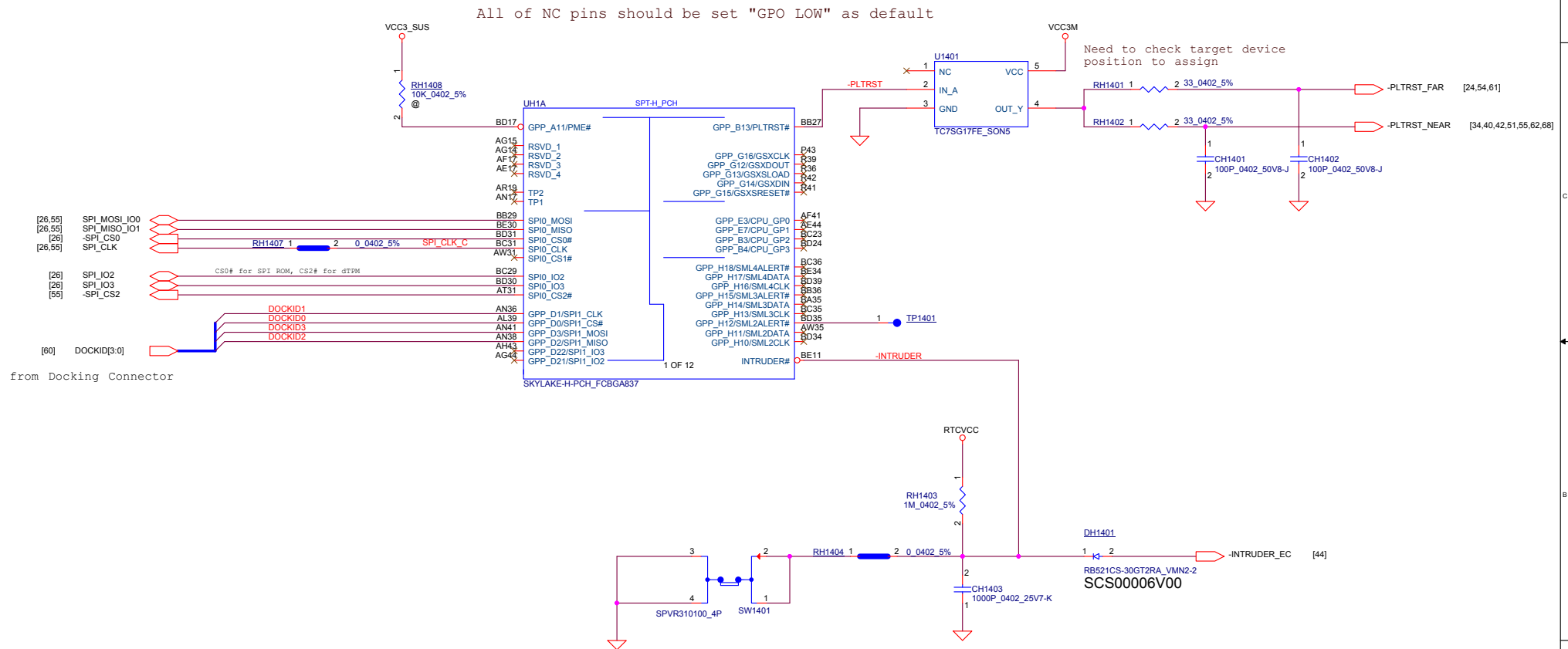
VDDQ DECOUPLING





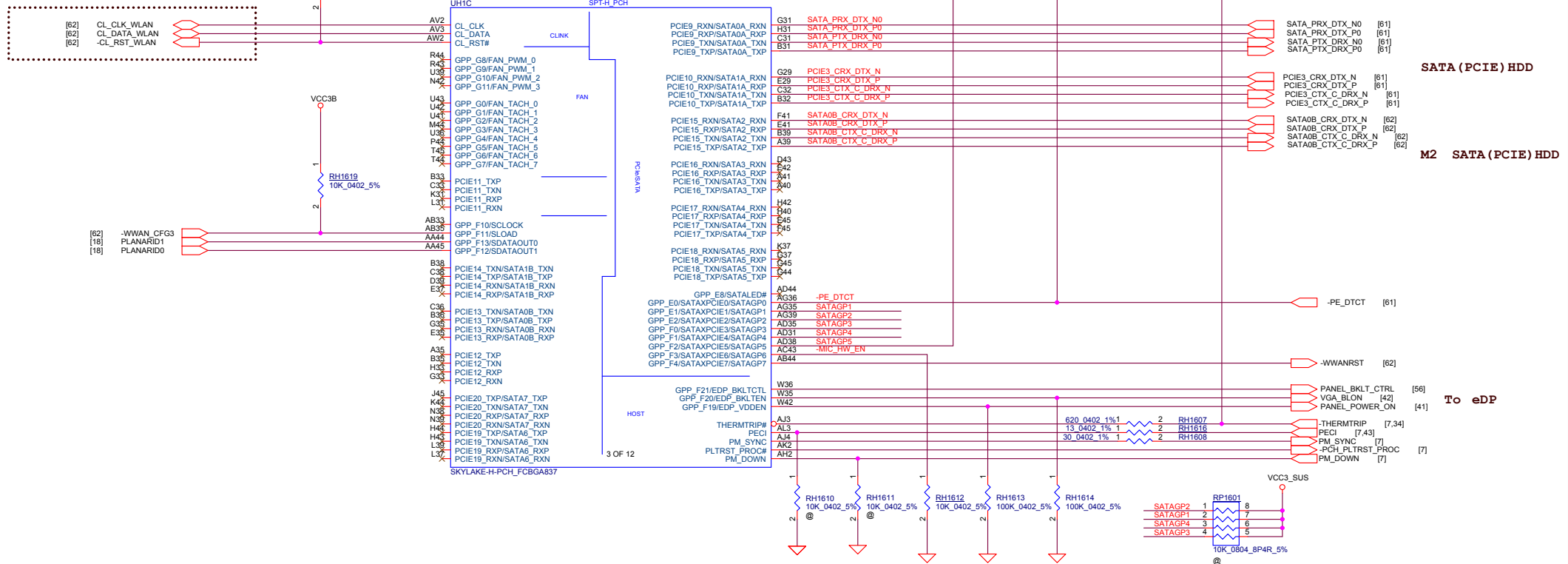
OPC_RCOM Support 4+4e
If not use can't conector





Flexible I/O	Port#	Configuration	Port Assignment
PCIe #20	26		
PCIe #19	25		
PCIe #18	24		
PCIe #17	23		
PCIe #16	22	SATA #3	M.2 Type B connector
PCIe #15	21	SATA #2	M.2 Type B connector
PCIe #14	20		
PCIe #13	19		
PCIe #12	18		
PCIe #11	17		
PCIe #10	16	PCIe #10	SATA-Express connector
PCIe #9	15	SATA #0/PCIe #9	SATA-Express connector
PCIe #8	14		
PCIe #7	13		
PCIe #6	12		
PCIe #5	11	PCIe #5	Cardreader
USB3 #10	10	PCIe #4	GbE PHY
USB3 #9	9		
USB3 #8	8		
USB3 #7	7	PCIe #1	WLAN
USB3 #6	6		
USB3 #5	5	USB3 #5	
USB3 #4	4	USB3 #4	Docking USB3.0 port
USB3 #3	3	USB3 #3	USB AOU port
USB3 #2	2	USB3 #2	USB Port 2
USB3 #1	1	USB3 #1	USB Port 1

from / to WLAN



Notes:

- The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
- SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
 - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
 - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

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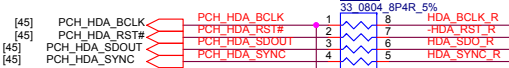
99

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TABLE : Functional Strap

HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME Regions of the SPI after MFG Done bit is set.



[45] PCH_HDA_BCLK

[45] PCH_HDA_RST#

[45] PCH_HDA_SDO0

[45] PCH_HDA_SDO1

[45] PCH_HDA_SYNC

[45] PCH_HDA_SYNC

[45] PCH_HDA_SYNC

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[45] PCH_HDA_SYNC

[45] PCH_HDA_SYNC

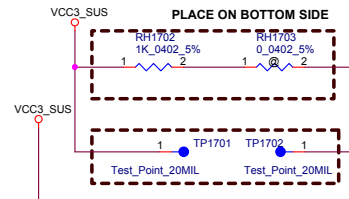
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[45] PCH_HDA_SYNC

[45] PCH_HDA_SYNC



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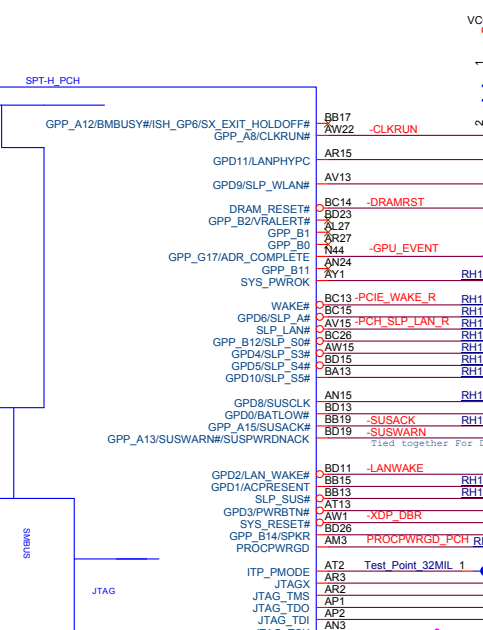
TEST PAD
BOTTOM SIDE
DO NOT MOVE AFTER FIX

TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS(Default)



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TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

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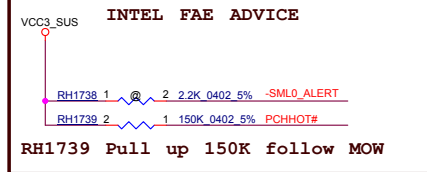
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RH1739 Pull up 150K follow MOW


RH1739 Pull up 150K follow MOW

RH1739 Pull up 150K follow MOW

RH1739 Pull up 150K follow MOW

RH1739 Pull up 150K follow MOW

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Issued Date	2015/07/16	Deciphered Date	2016/01/16
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Title			
PCH SKL-H : AUDIO/SMBUS/JTAG			
Size	Document Number	Rev	
Custom		0.1	
Date: Tuesday, November 03, 2015		Sheet 17 of 99	
		NM-A611	

Rev 0.1

Rev 0.1

Rev 0.1

Rev 0.1

to be confirm on SDV

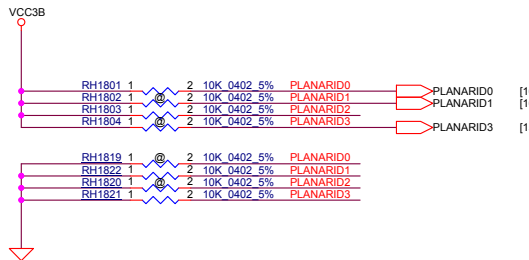
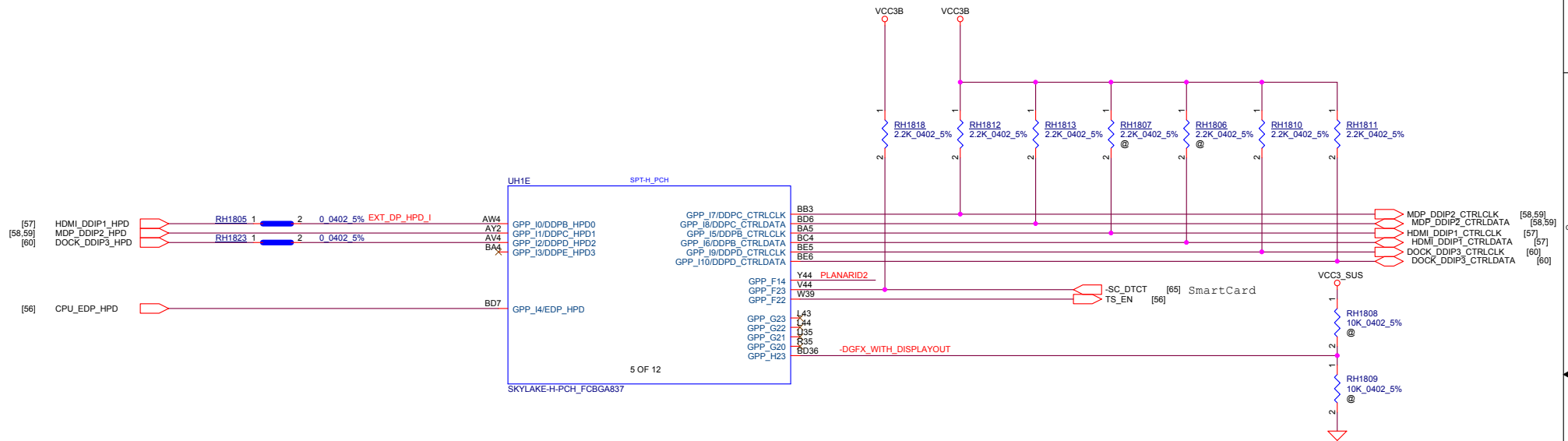
RH1816 1 2 100K 0.402 5% HDMI_DDIP1_HPD

RH1814 NODPRE@1 1 2 100K 0.402 5% MDP_DDIP2_HPD


RH1817 1 2 100K 0.402 5% DOCK_DDIP3_HPD

RH1815 1 2 100K 0.402 5% CPU_EDP_HPD

DDIP2_HPD : PS8330 has Int.PD 150K



	PLANAR ID			
	3	2	1	0
SDV	0	0	0	0
FVT	0	0	0	1
FVT2	0	0	1	0
SIT	0	0	1	1
SWG FVT	0	1	0	0
SWG SIT UMA SVT	0	1	0	1

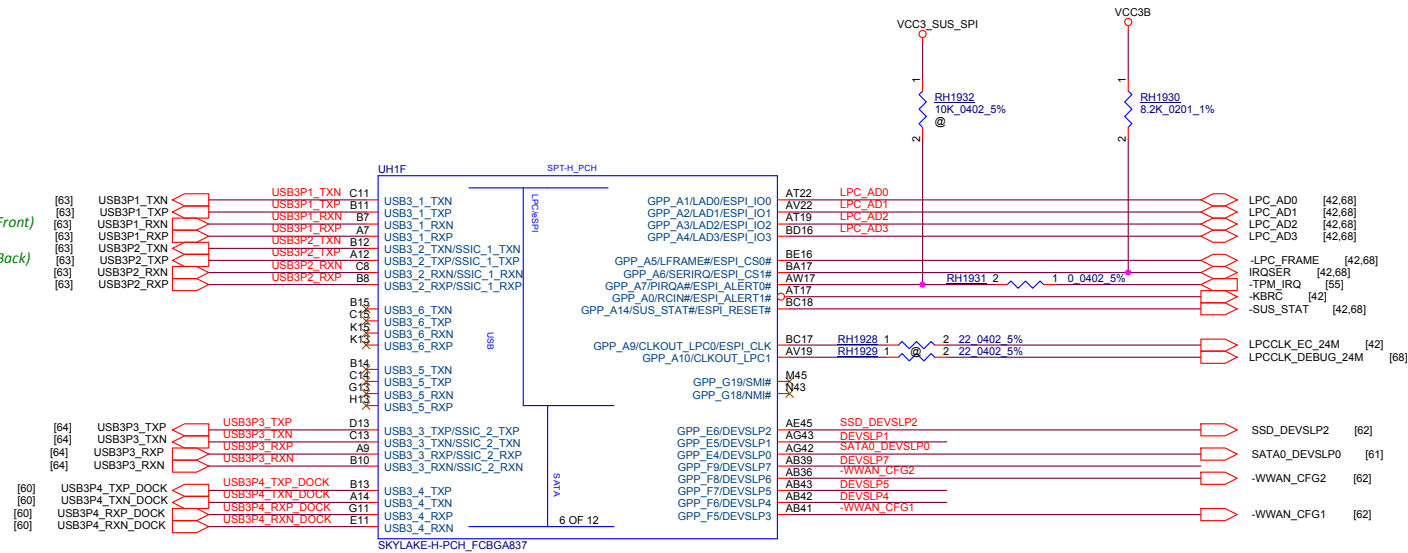
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/07/16	Deciphered Date	2016/01/16	PCH SKL-H : DDI CONTROL		
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				Date:	Tuesday, November 03, 2015	Sheet 18 of 99 Rev 0.1

System Port 1 (Right-Front)

System Port 2 (Right-Back)

Small Board

DOCKING



[7] CPU_REFCLK_24M
[7] -CPU_REFCLK_24M
[7] CPU_BCLK_100M
[7] -CPU_BCLK_100M

VCC1R0_SUS

RH2005 1 2 2.7K 0402 0.5%

[62] CLKREQ_PCIE0_WLAN#
[61] CLKREQ_PCIE1_SATA#

[51] CLKREQ_PCIE3_LAN#
[54] CLKREQ_PCIE4_CR#
[31] CLKREQ_PCIE5_VGA#

VCC3B

RP2001

1 2 3 4

8 7 6 5

CLKREQ_PCIE0_WLAN#

CLKREQ_PCIE1_SATA#

CLKREQ_PCIE3_LAN#

10K_0804_8P4R_5%

RH2012 1 2 10K 0402 5%

RH2018 1 2 10K 0402 5%

CLKREQ_PCIE4_CR#

CLKREQ_PCIE5_VGA#

RP2002

1 2 3 4

8 7 6 5

CLKREQ_PCIE0_WLAN#

CLKREQ_PCIE1_SATA#

CLKREQ_PCIE3_LAN#

10K_0804_8P4R_5%

RH2015 1 2 10K 0402 5%

RH2013 1 2 10K 0402 5%

CLKREQ_PCIE4_CR#

CLKREQ_PCIE5_VGA#

CH2001

15P_0402_50V8-J

1 2

RTCX1

Y2001

32.768KHZ_12.5PF_9H03200042

1 2

RTCX2

CH2002

15P_0402_50V8-J

1 2

Y1 ->

KDS

17JH090DR1A0001

CH2003

3.9P_0402_50V8-B

1 2

XTAL24_OUT

24MHZ_6PF_8Y24000010

Y2002

4 2

XTAL24_IN

CH2004

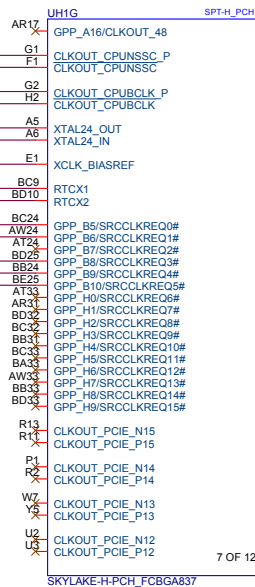
3.9P_0402_50V8-B

1 2

Y1 ->

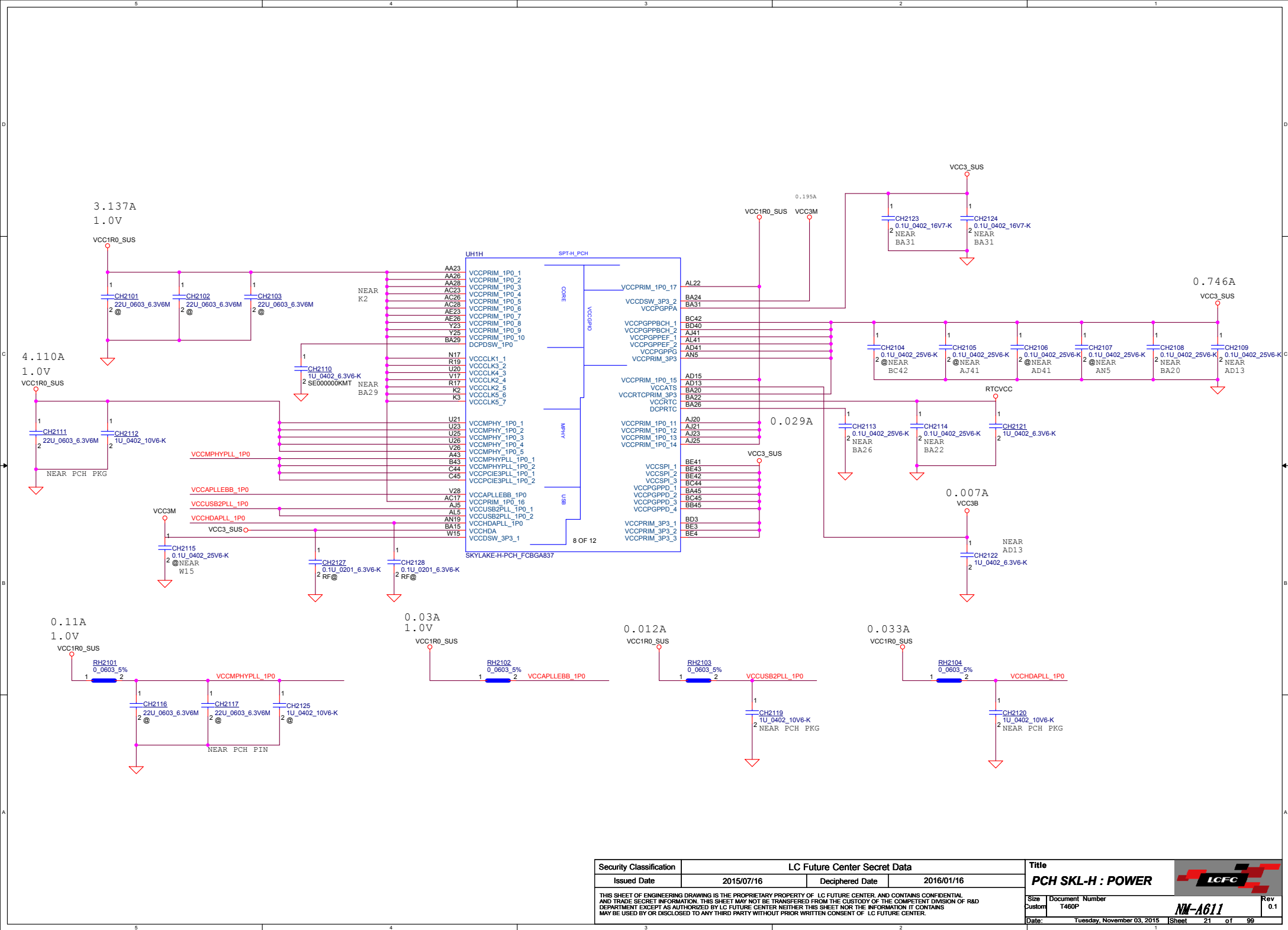
TXC


8Y24000010



PCIE Clock Assignment
Clock 0 : WLAN
Clock 1 : SATA
Clock 3 : Giga LAN
Clock 4 : CARD READER
Clock 5 : GPU N16S-GT

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Issued Date	2015/07/16	Deciphered Date	2016/01/16	PCH SKL-H : CLK
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Date: Tuesday, November 03, 2015				Rev 0.1 Sheet 20 of 99



Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		PCH SKL-H : POWER			
2015/07/16		2016/01/16		Size Document Number T460P		Rev 0.1 NW-A611	
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UH1I SPT-H_PCH

AC18	VSS_1	VSS_76	AR5
AN4	VSS_2	VSS_76	AR7
AN10	VSS_3	VSS_77	U15
BE14	VSS_4	VSS_78	AL4
BE18	VSS_5	VSS_79	AE29
BE23	VSS_6	VSS_80	AE4
BE28	VSS_7	VSS_81	AE42
BE32	VSS_8	VSS_82	AF18
BE37	VSS_9	VSS_83	AF20
BE40	VSS_10	VSS_84	AF21
BE9	VSS_11	VSS_85	AF23
C10	VSS_12	VSS_86	AF25
C2	VSS_13	VSS_87	AF26
C28	VSS_14	VSS_88	AF28
C37	VSS_15	VSS_89	AF29
J7	VSS_16	VSS_90	AG11
K10	VSS_17	VSS_91	AG13
K27	VSS_18	VSS_92	AG31
K33	VSS_19	VSS_93	AG32
K36	VSS_20	VSS_94	AG33
K4	VSS_21	VSS_95	AG38
K42	VSS_22	VSS_96	AG4
K43	VSS_23	VSS_97	AH1
L12	VSS_24	VSS_98	AH17
L13	VSS_25	VSS_99	AH18
L15	VSS_26	VSS_100	AH20
L4	VSS_27	VSS_101	AH21
L41	VSS_28	VSS_102	AH23
L8	VSS_29	VSS_103	AH26
M35	VSS_30	VSS_104	AH28
M42	VSS_31	VSS_105	AH29
N10	VSS_32	VSS_106	AH35
N15	VSS_33	VSS_107	AJ10
N22	VSS_34	VSS_108	AJ14
N24	VSS_35	VSS_109	AJ15
N35	VSS_36	VSS_110	AJ17
N36	VSS_37	VSS_111	AJ18
N4	VSS_38	VSS_112	AJ26
N41	VSS_39	VSS_113	AJ28
N5	VSS_40	VSS_114	AJ29
P17	VSS_41	VSS_115	AJ31
P19	VSS_42	VSS_116	AJ32
P22	VSS_43	VSS_117	AJ36
P45	VSS_44	VSS_118	AK4
R10	VSS_45	VSS_119	AK42
R14	VSS_46	VSS_120	AU7
R22	VSS_47	VSS_121	AV17
R29	VSS_48	VSS_122	AV24
R33	VSS_49	VSS_123	AV27
R38	VSS_50	VSS_124	AV31
R5	VSS_51	VSS_125	AV33
T1	VSS_52	VSS_126	AV6
T4	VSS_53	VSS_127	AW13
Y18	VSS_54	VSS_128	AW19
Y20	VSS_55	VSS_129	AW27
Y21	VSS_56	VSS_130	AW37
Y26	VSS_57	VSS_131	AW9
Y28	VSS_58	VSS_132	AY38
Y29	VSS_59	VSS_133	AY45
Y29	VSS_60	VSS_134	B25
A18	VSS_61	VSS_135	B3
A25	VSS_62	VSS_136	B37
A32	VSS_63	VSS_137	B40
A37	VSS_64	VSS_138	B6
AA17	VSS_65	VSS_139	BA1
AA18	VSS_66	VSS_140	BE11
AA20	VSS_67	VSS_141	BB16
AA21	VSS_68	VSS_142	BB21
AA25	VSS_69	VSS_143	BB25
AA29	VSS_70	VSS_144	BB30
AA4	VSS_71	VSS_145	BB34
AA42	VSS_72	VSS_146	BC2
AB10	VSS_73	VSS_147	BD43
AB10	VSS_74	VSS_148	

9 OF 12
SKYLAKE-H-PCH_FCBGA837

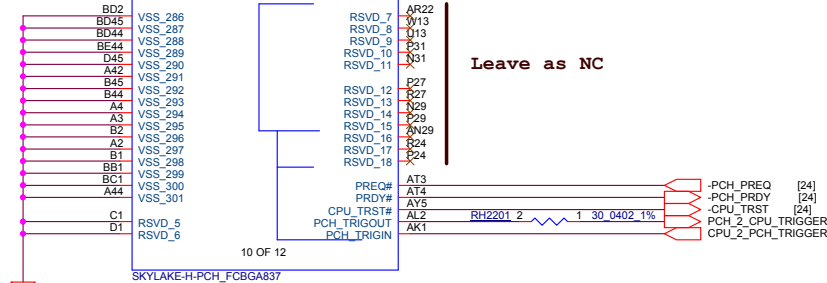
UH1L SPT-H_PCH

C42	VSS_149	VSS_217	AB11
D10	VSS_150	VSS_218	AB7
D12	VSS_151	VSS_219	AB14
D15	VSS_152	VSS_220	AB31
AE29	VSS_153	VSS_221	AB32
D17	VSS_154	VSS_222	AB38
AE42	VSS_155	VSS_223	AB4
D21	VSS_156	VSS_224	AB5
D24	VSS_157	VSS_225	AC1
AF21	VSS_158	VSS_226	AC20
AF23	VSS_159	VSS_227	AC21
D29	VSS_160	VSS_228	AC25
D30	VSS_161	VSS_229	AC29
D31	VSS_162	VSS_230	AC45
D33	VSS_163	VSS_231	AC8
D36	VSS_164	VSS_232	AD11
AG13	VSS_165	VSS_233	AD14
AG31	VSS_166	VSS_234	AB15
E13	VSS_167	VSS_235	AD32
E15	VSS_168	VSS_236	AD33
E31	VSS_169	VSS_237	AD38
AG38	VSS_170	VSS_238	AD4
F44	VSS_171	VSS_239	AD8
F8	VSS_172	VSS_240	AE18
G42	VSS_173	VSS_241	AE20
G9	VSS_174	VSS_242	AE21
H17	VSS_175	VSS_243	AE25
H19	VSS_176	VSS_244	AE28
H22	VSS_177	VSS_245	AL10
H24	VSS_178	VSS_246	AL11
H27	VSS_179	VSS_247	AL13
H28	VSS_180	VSS_248	AL17
H3	VSS_181	VSS_249	AL19
H35	VSS_182	VSS_250	AL24
J10	VSS_183	VSS_251	AL29
J11	VSS_184	VSS_252	AL32
J15	VSS_185	VSS_253	AL33
J39	VSS_186	VSS_254	AL38
J5	VSS_187	VSS_255	AM15
J42	VSS_188	VSS_256	AM17
U10	VSS_189	VSS_257	AM19
U11	VSS_190	VSS_258	AM22
U14	VSS_191	VSS_259	AM24
U17	VSS_192	VSS_260	AM27
U18	VSS_193	VSS_261	AM29
U28	VSS_194	VSS_262	AM45
U29	VSS_195	VSS_263	AN11
U31	VSS_196	VSS_264	AN22
U32	VSS_197	VSS_265	AN27
U33	VSS_198	VSS_266	AN31
U38	VSS_199	VSS_267	AN39
U4	VSS_200	VSS_268	AN7
U4	VSS_201	VSS_269	AN8
U8	VSS_202	VSS_270	AP11
V21	VSS_203	VSS_271	AP4
V23	VSS_204	VSS_272	AR33
V25	VSS_205	VSS_273	AR34
V29	VSS_206	VSS_274	AR42
V3	VSS_207	VSS_275	AR9
V45	VSS_208	VSS_276	AT10
W14	VSS_209	VSS_277	AT15
W31	VSS_210	VSS_278	AT36
W32	VSS_211	VSS_279	AU1
W33	VSS_212	VSS_280	AU35
W38	VSS_213	VSS_281	AU36
W4	VSS_214	VSS_282	AU39
W6	VSS_215	VSS_283	AU45
Y17	VSS_216	VSS_284	C4
		VSS_285	

12 OF 12

SKYLAKE-H-PCH_FCBGA837

UH1J SPT-H_PCH



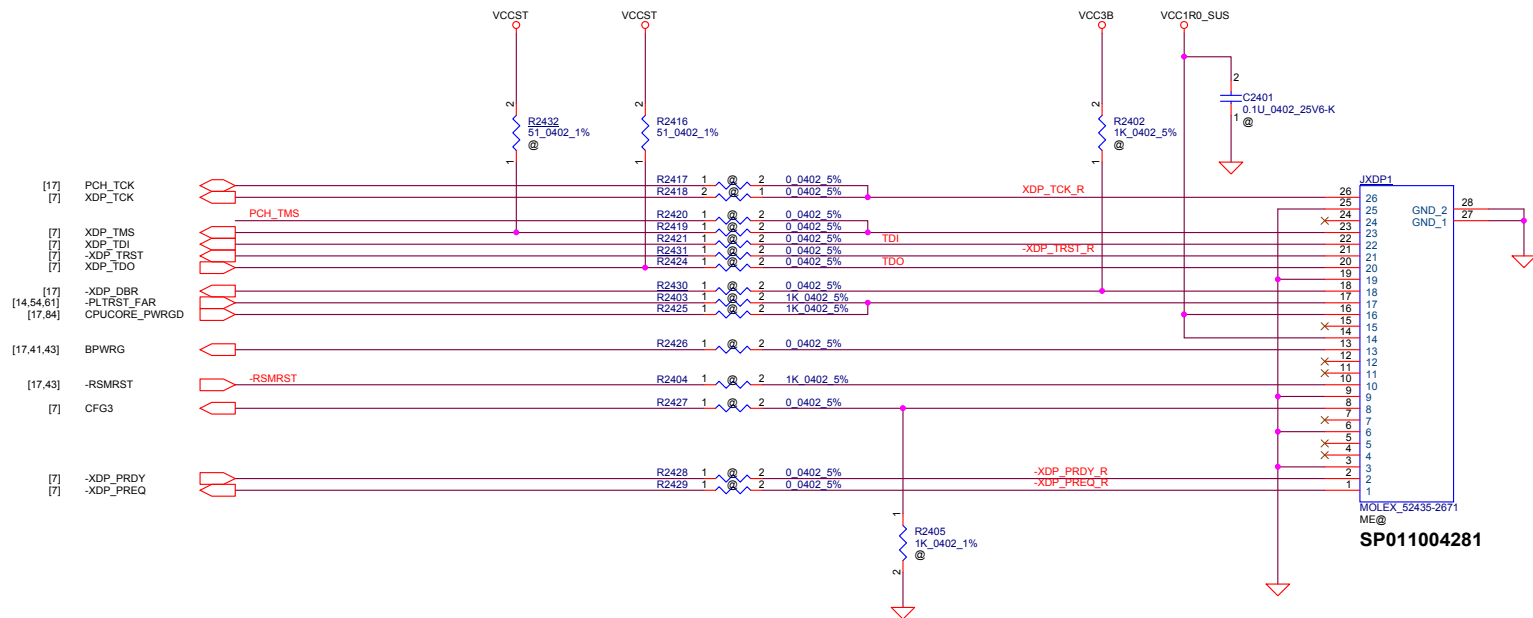
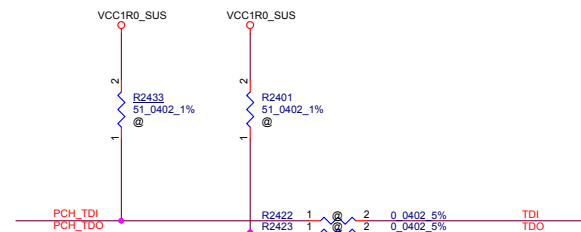
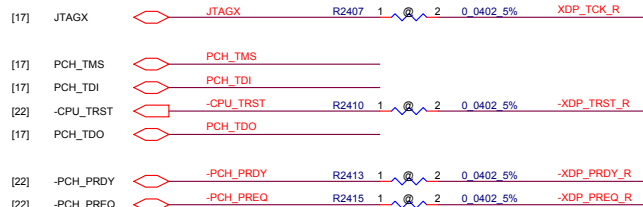
MOLEX_52435-2671
ME@
SP011004281

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

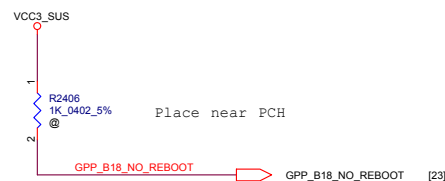
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	R2406
HIGH Enable "No Reboot" Mode	ASM
LOW Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

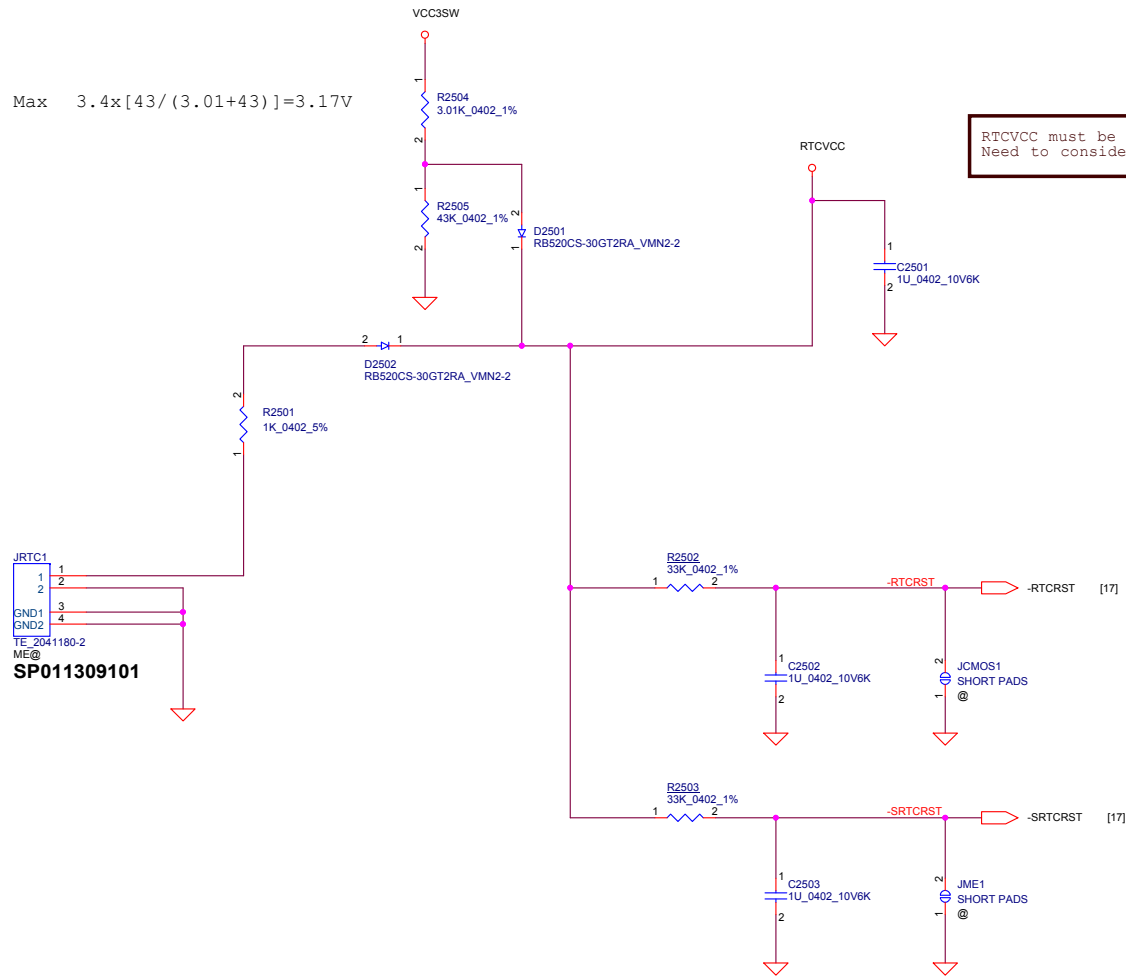


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					Document Number T460P
					Date: Tuesday, November 03, 2015
					Sheet 24 of 99
					Rev 0.1

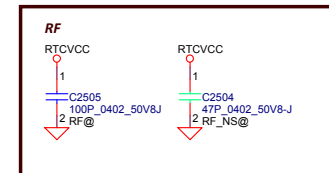


NM-A611

$$\text{Max } 3.4 \times [43 / (3.01 + 43)] = 3.17\text{V}$$

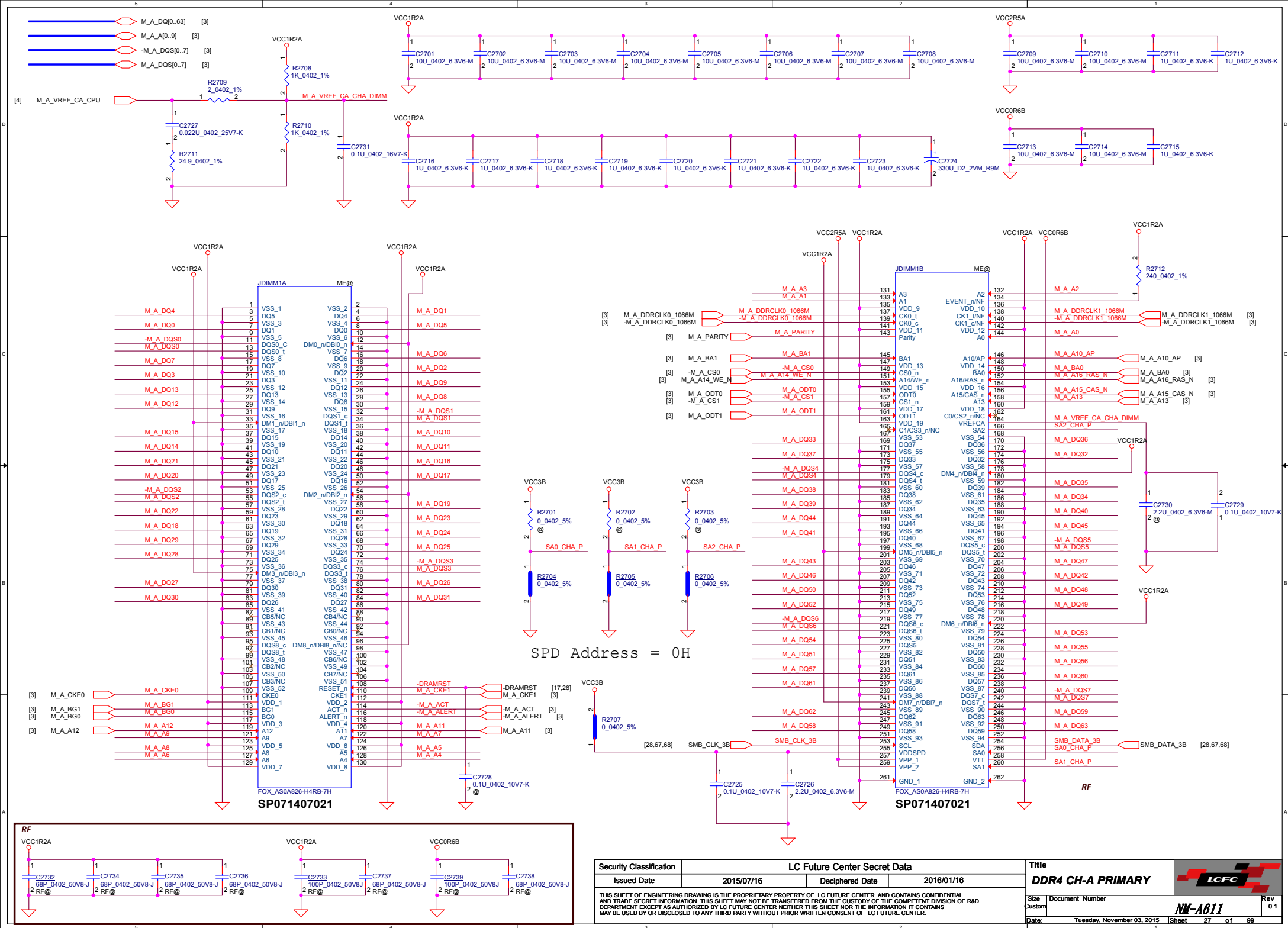


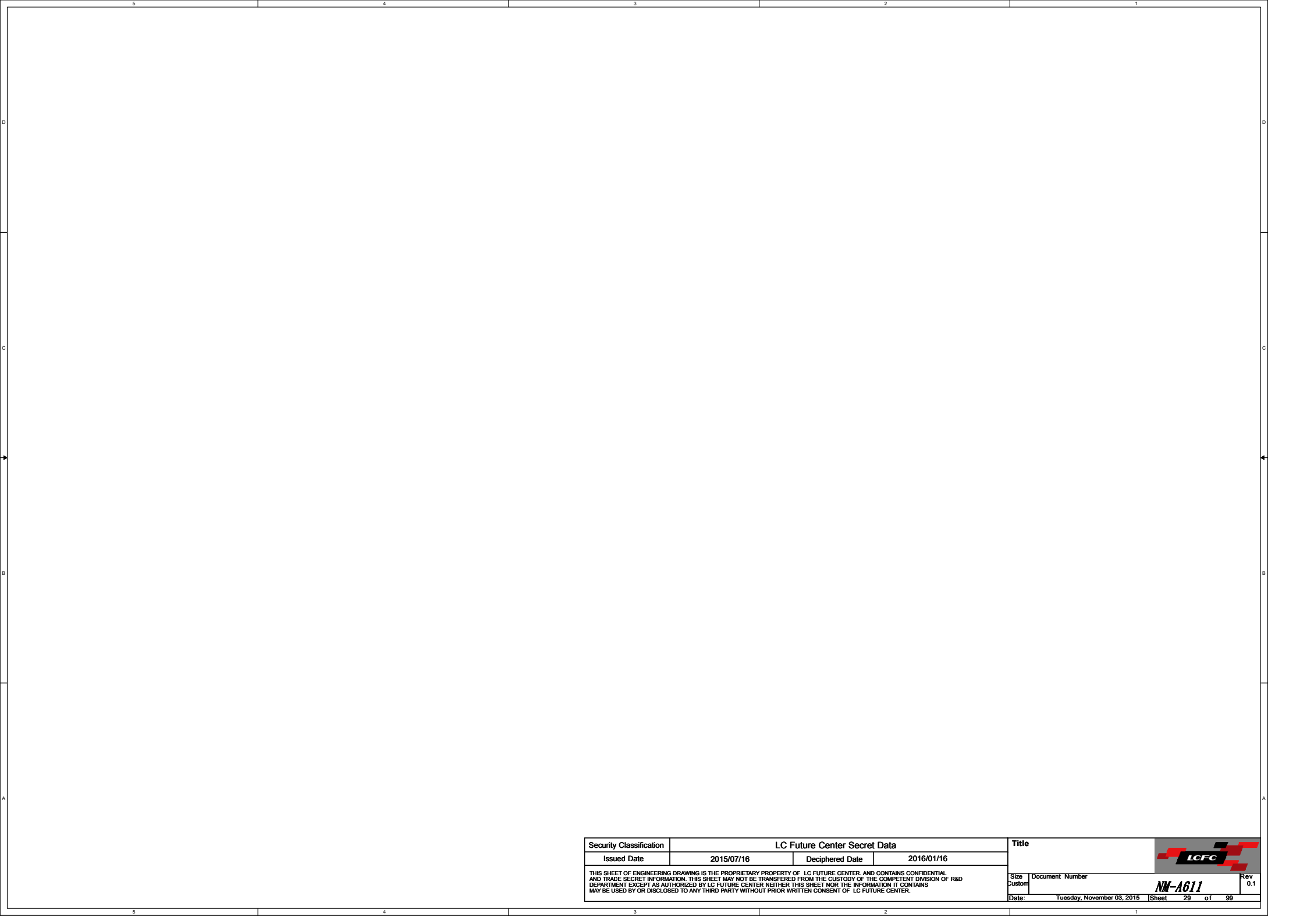
RTCVCC must be less than 3.2V from SKL.
Need to consider voltage divider etc.




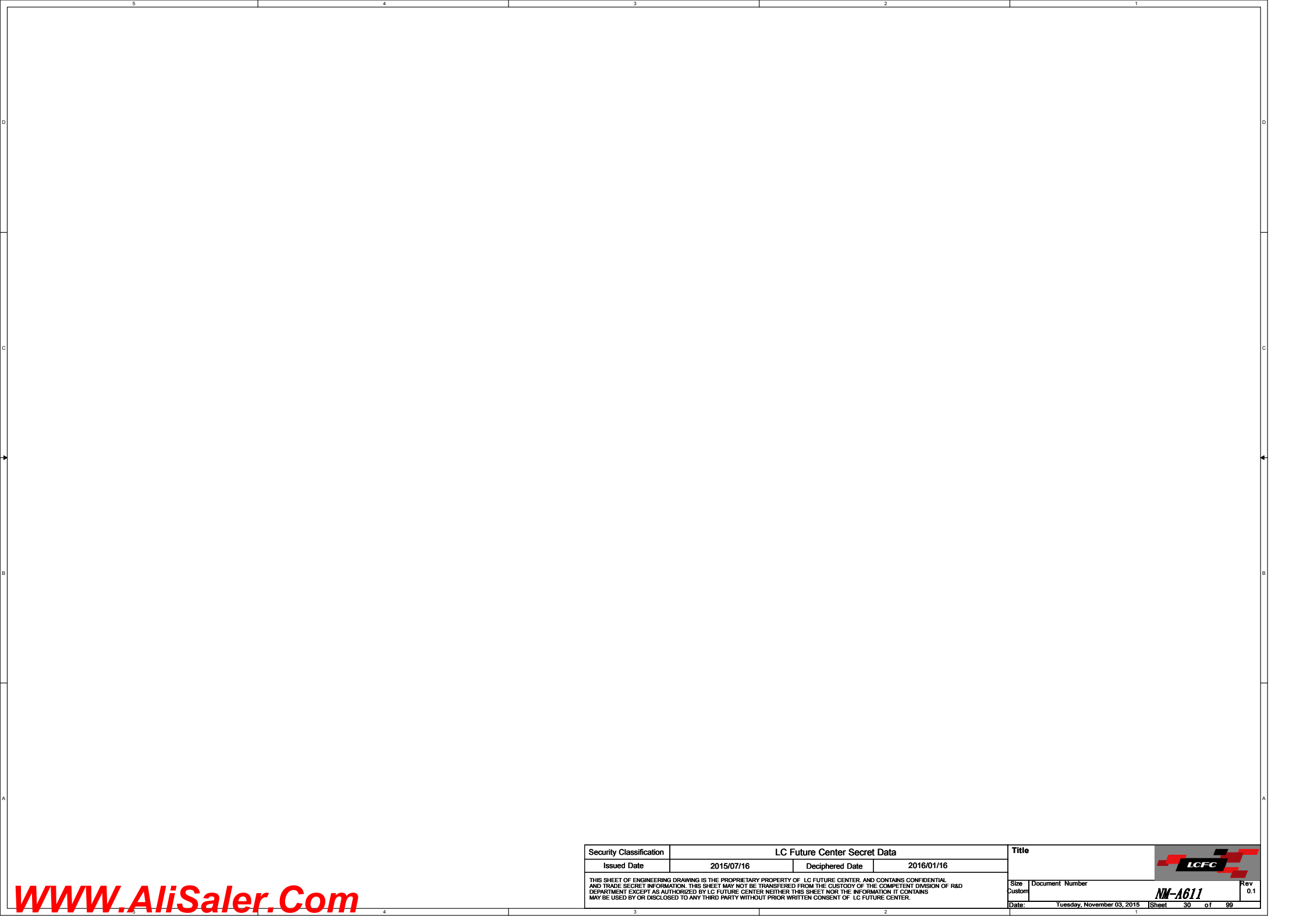
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					Document Number
					Rev 0.1
					Date: Tuesday, November 03, 2015




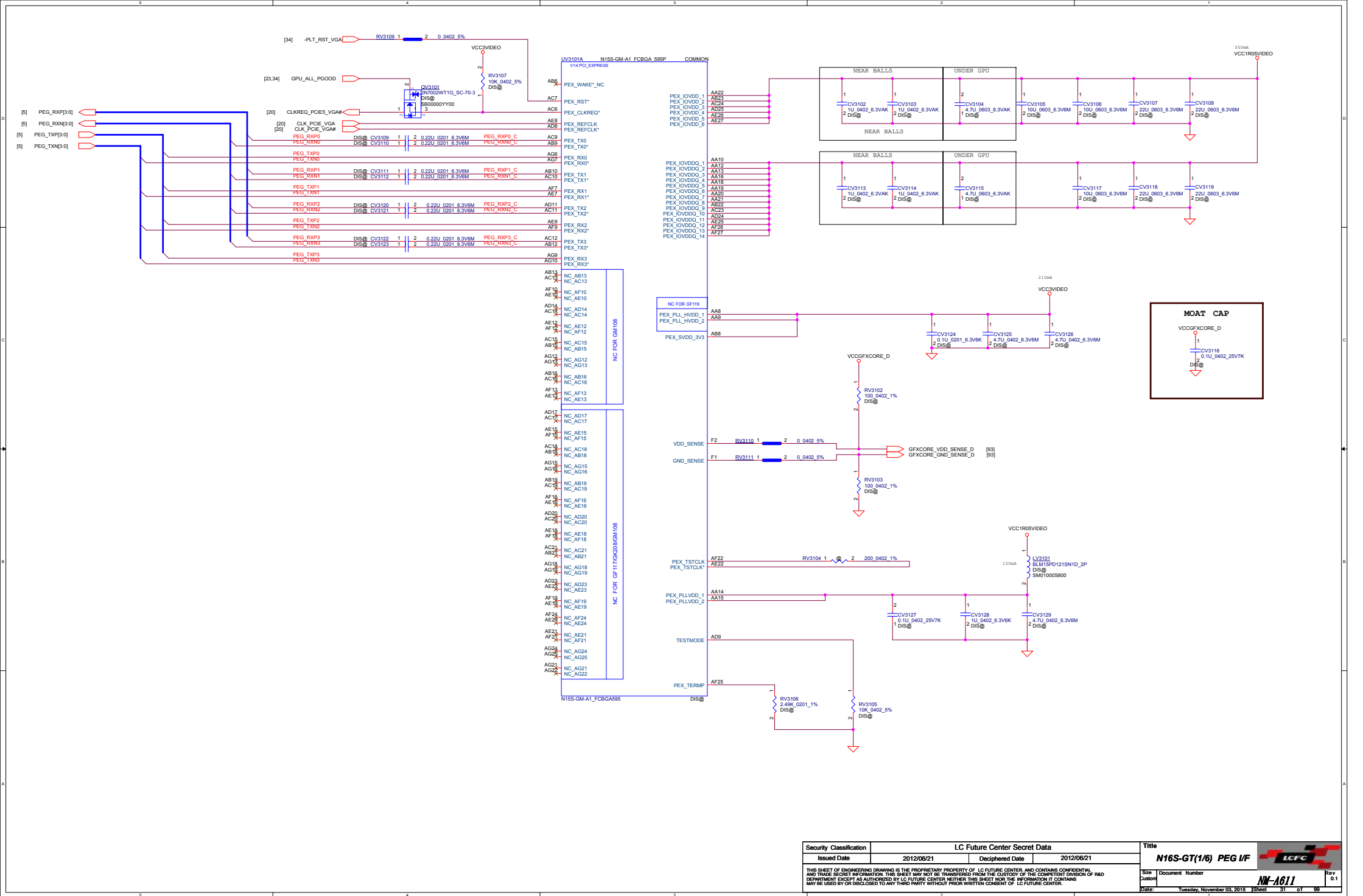


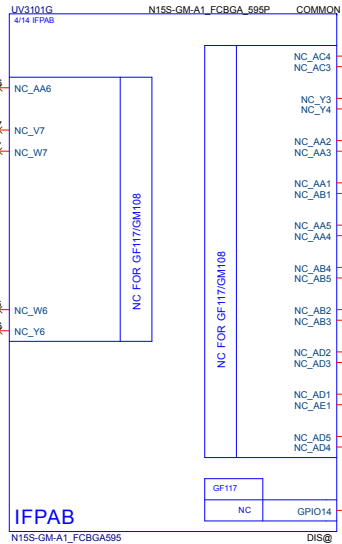


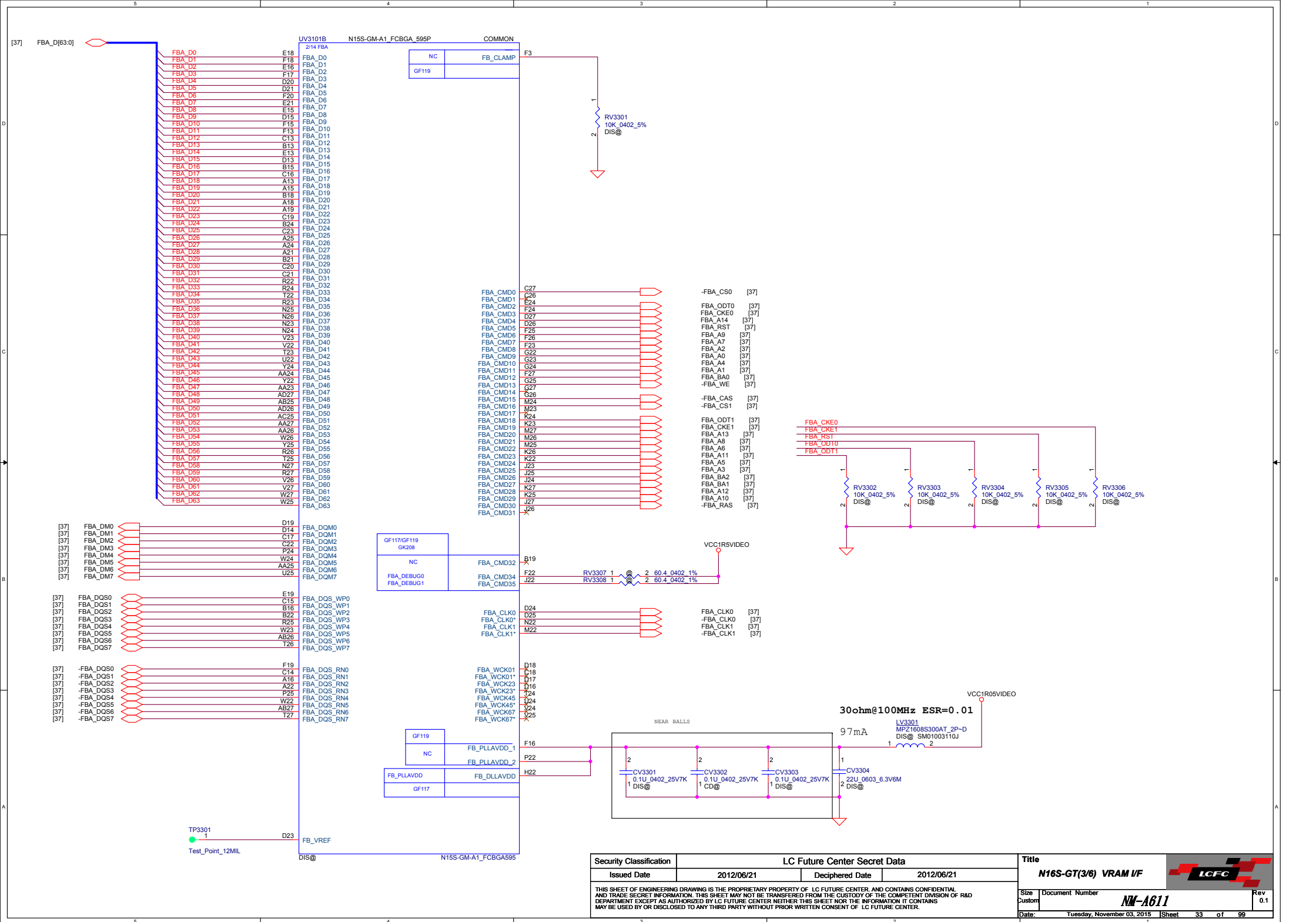
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				Date:	Tuesday, November 03, 2015	Sheet 29 of 99

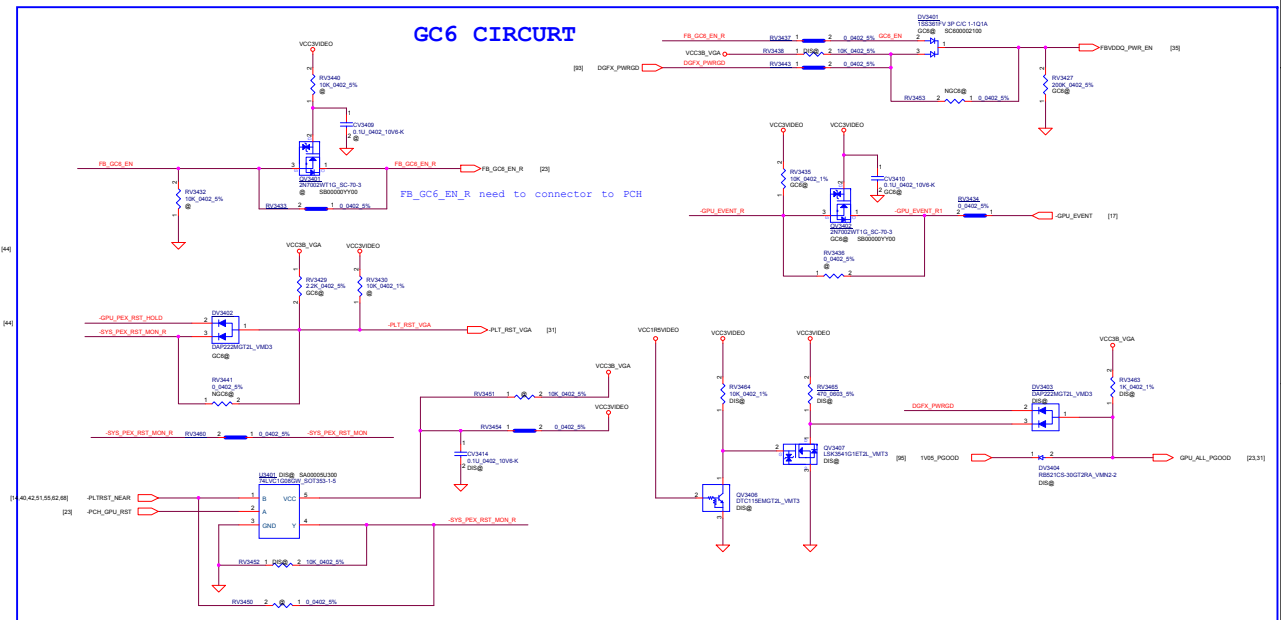
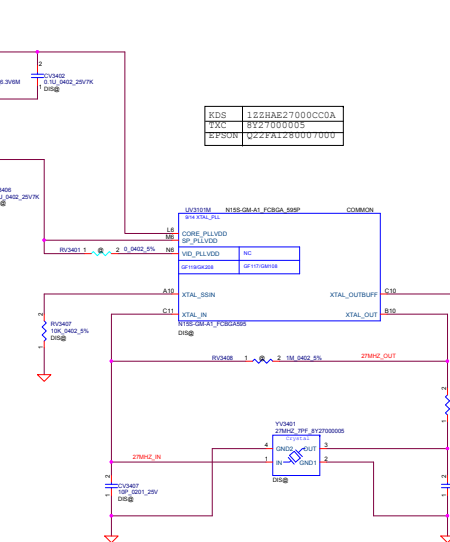
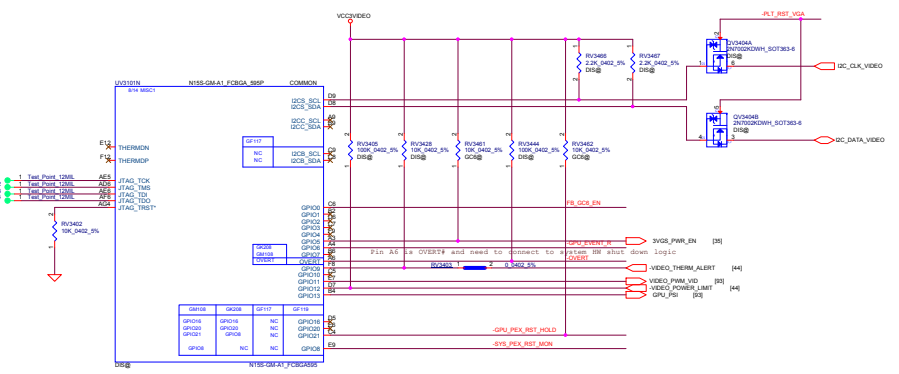


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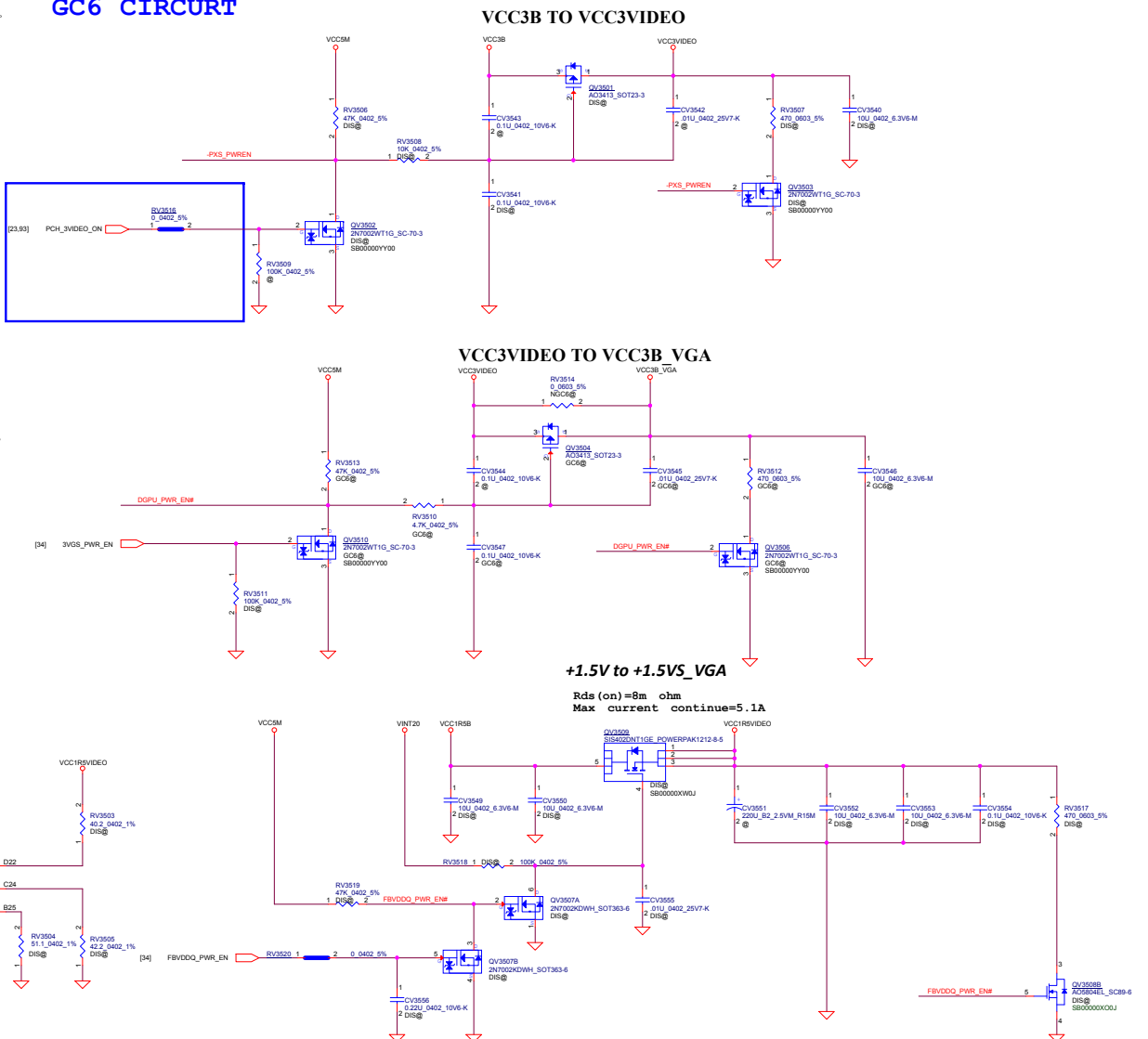
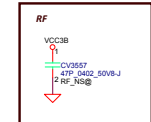
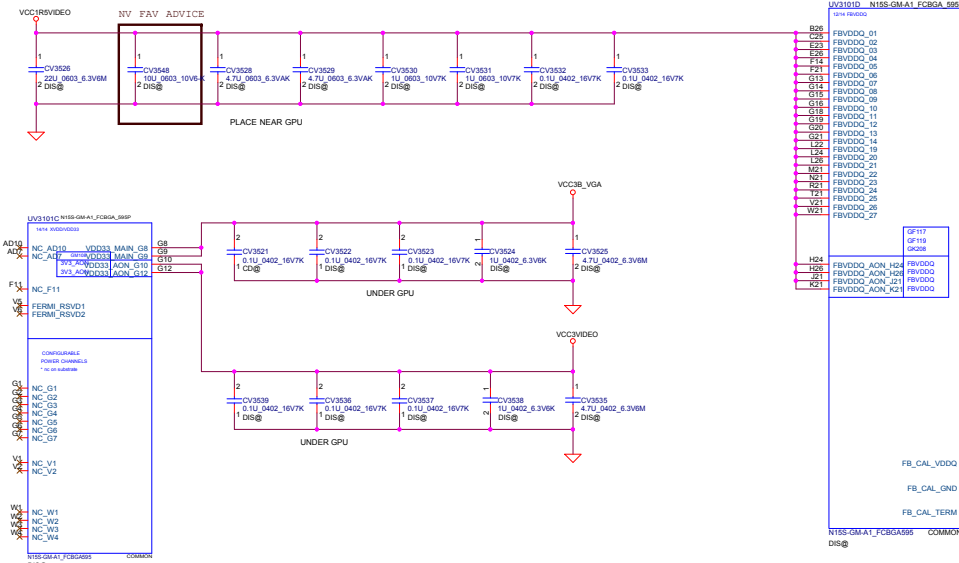
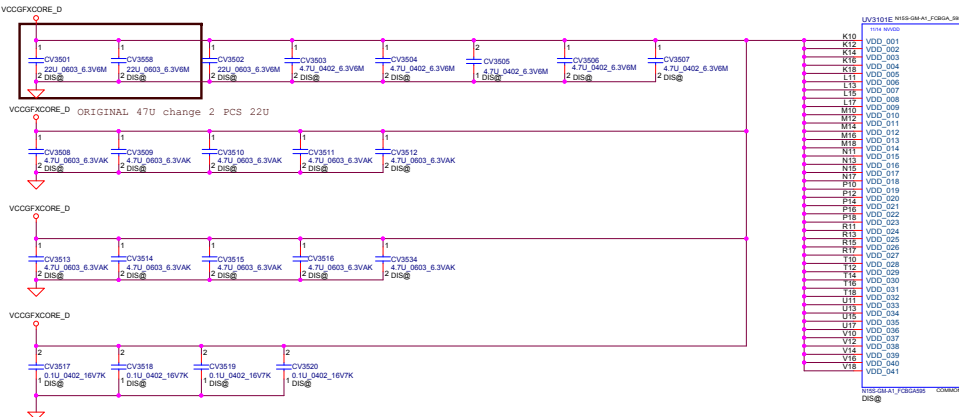


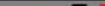
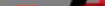


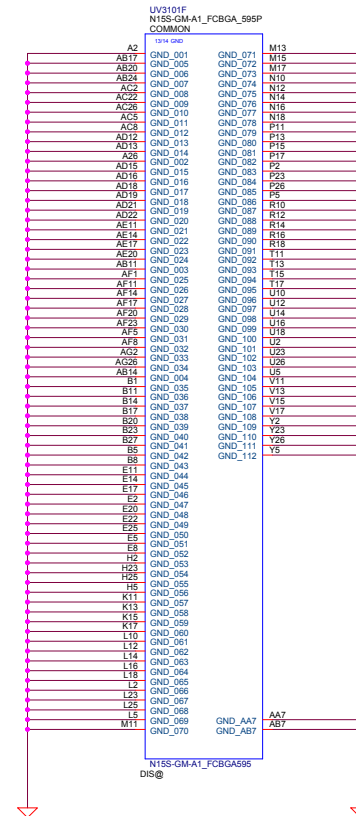



WWW.AliSaler.Com

GC6 CIRCURT

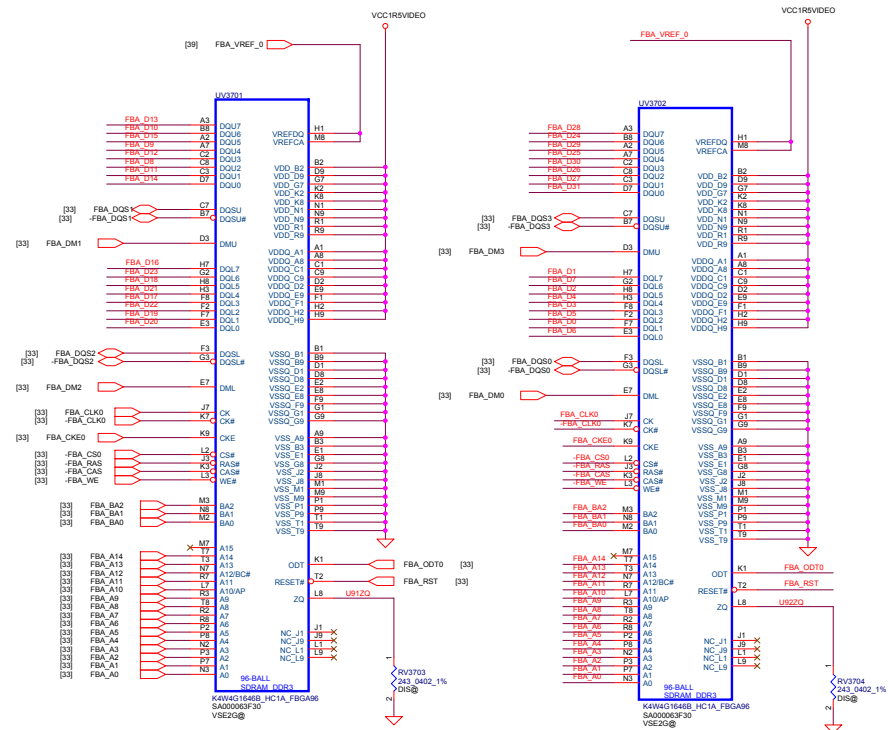
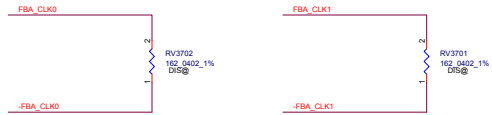


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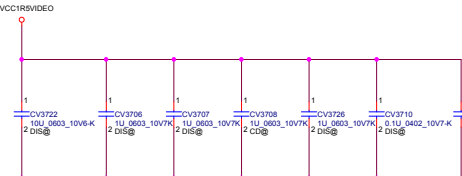


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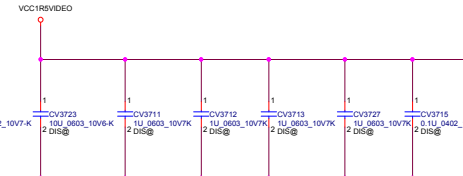
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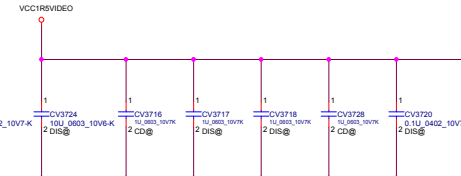
For UV3702
CLOSE TO THE MEMORY



For UV3703
CLOSE TO THE MEMORY





For UV3704
CLOSE TO THE MEMORY



TABLE

DDR3 VIDEO MEMORY					
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UV3701 UV3702 UV3703 UV3704	MT41J256M16HA-093G-E(E-Die) 256Mx16 SA000060100 -	H5TC4G63AFR-11C 256Mx16 SA00005YL10 -	K4W4G1646D-BC1A (D-Die)256Mx16 SA000063F00 -	K4W4G1646E-BC1A (D-Die)256Mx16(LCFC USE) SA000063F30 -	H5TC4G63CFR-N0C(C-Die) 256Mx16(LCFC USE) SA00007DU00 -
BOM Structure	VME2G@	VHA2G@	VSD2G@	VSE2G@	VHC2G@

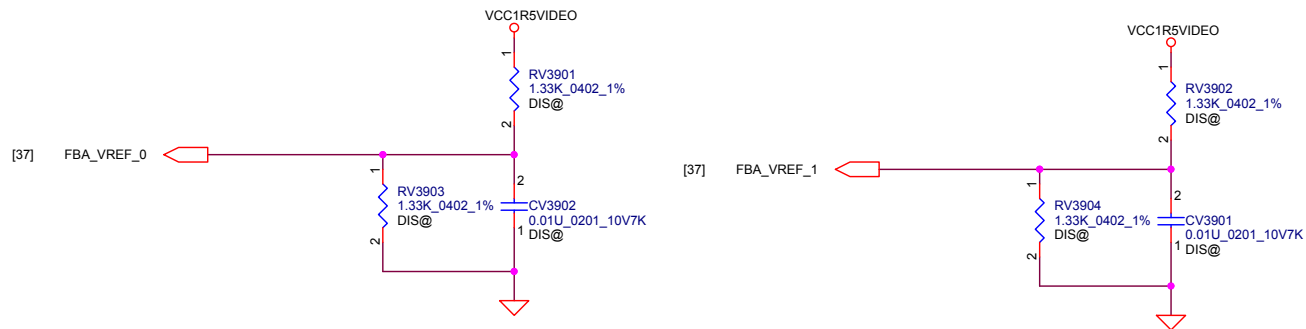
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		Page	1 of 1



HW-4811



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3		NM-A611		Sheet 39 of 99			

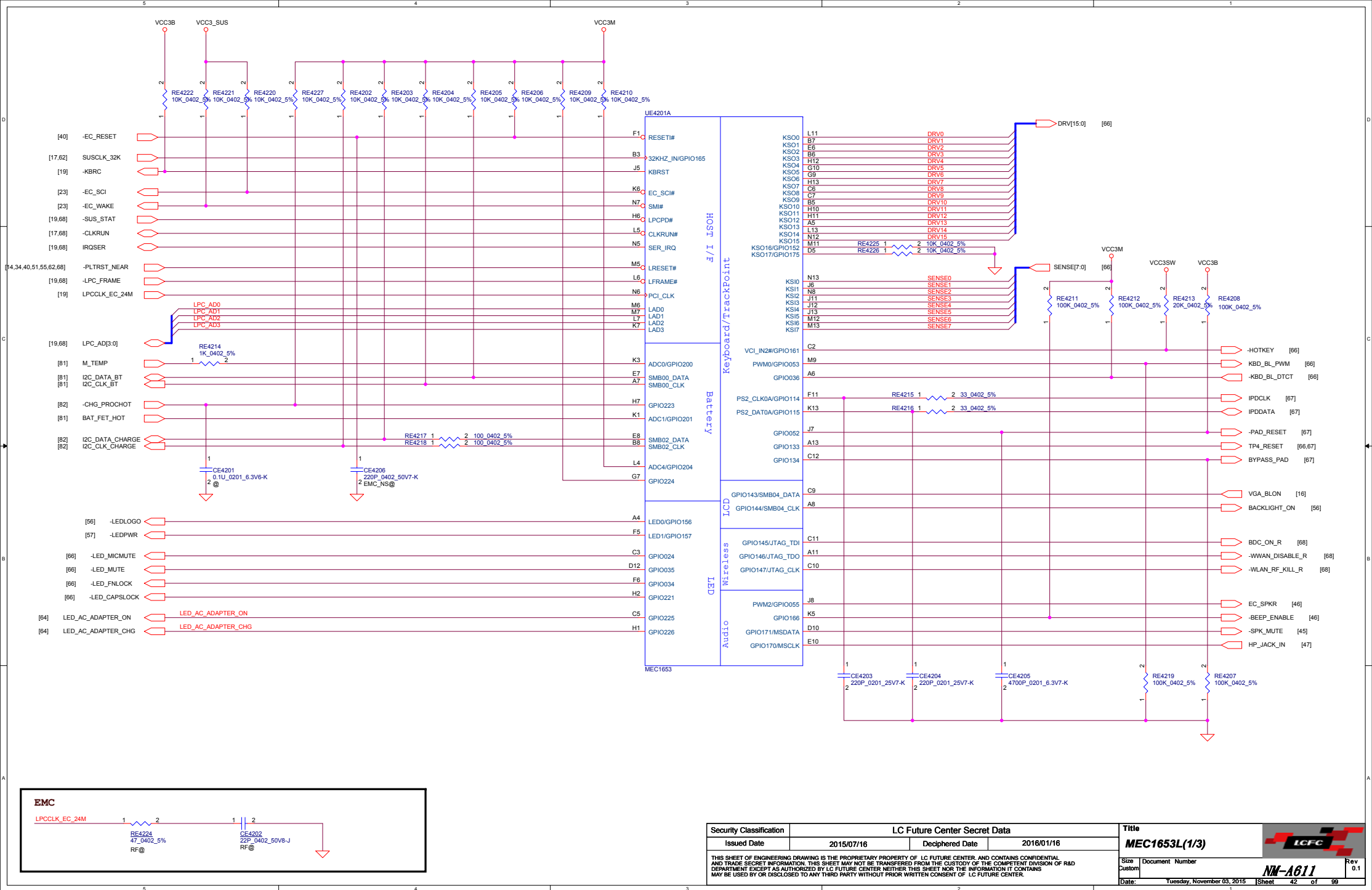
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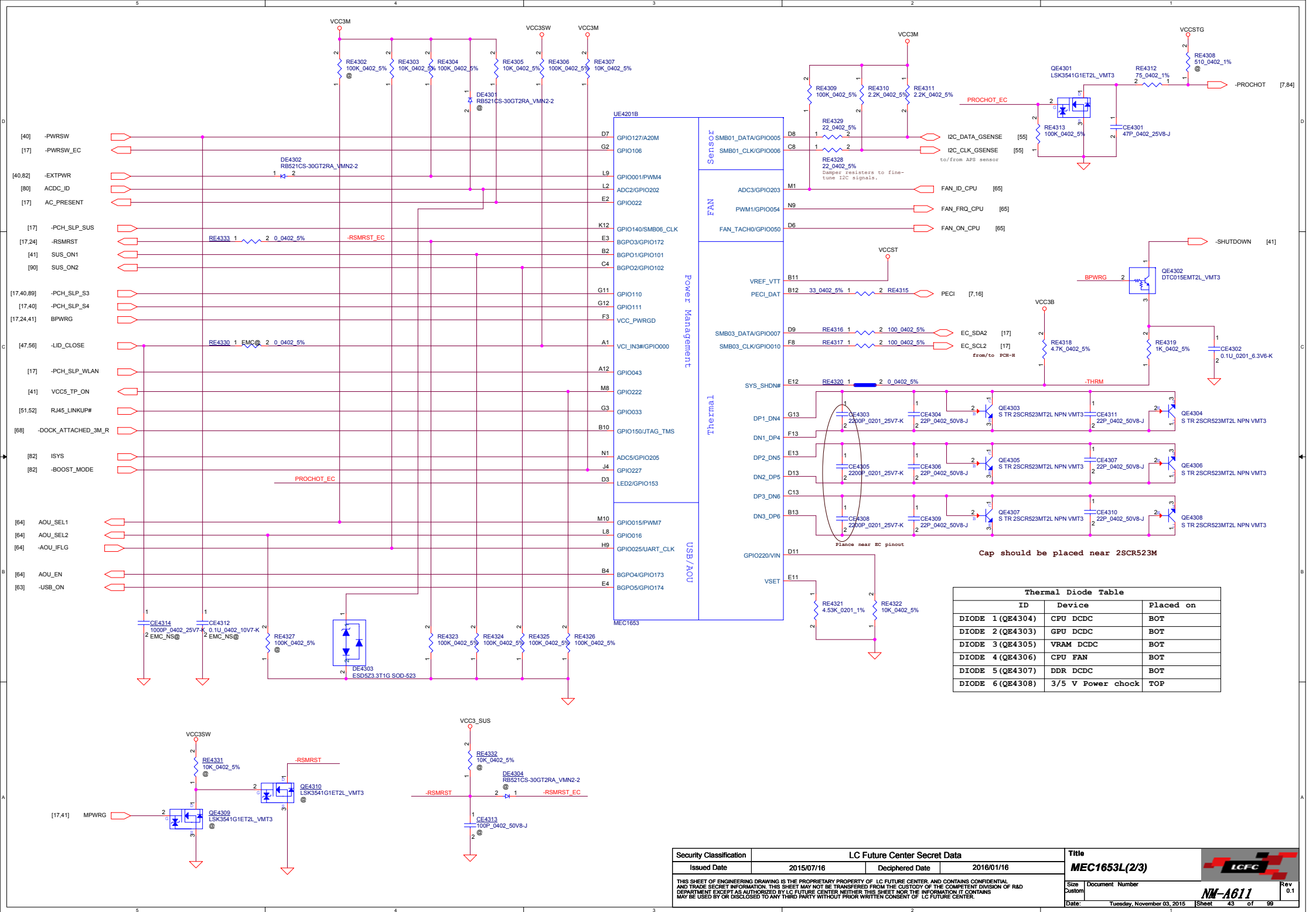
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RT4104	PQ10	M_BAT_PWR FET
RT4105	PQ601	VCCGFXCORE_D FET
RT4106	Q6001	DOCK_PWR FET (EE)
RT4107	PQ2	DCIN20_PWR FET
RT4112	PQ301	DDR_PWR FET
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RT4109	RESEVER	
RT4111	RESEVER	

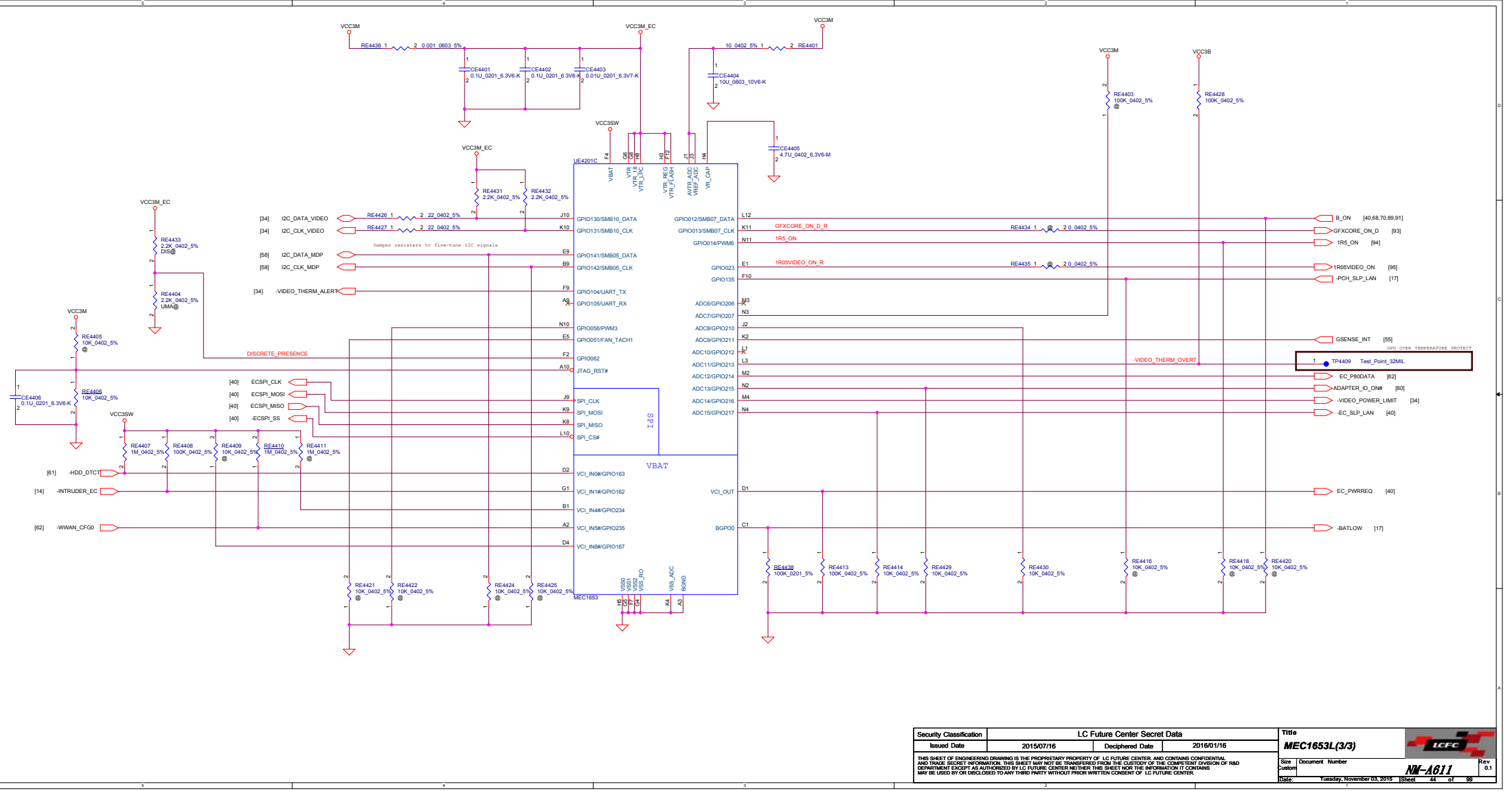
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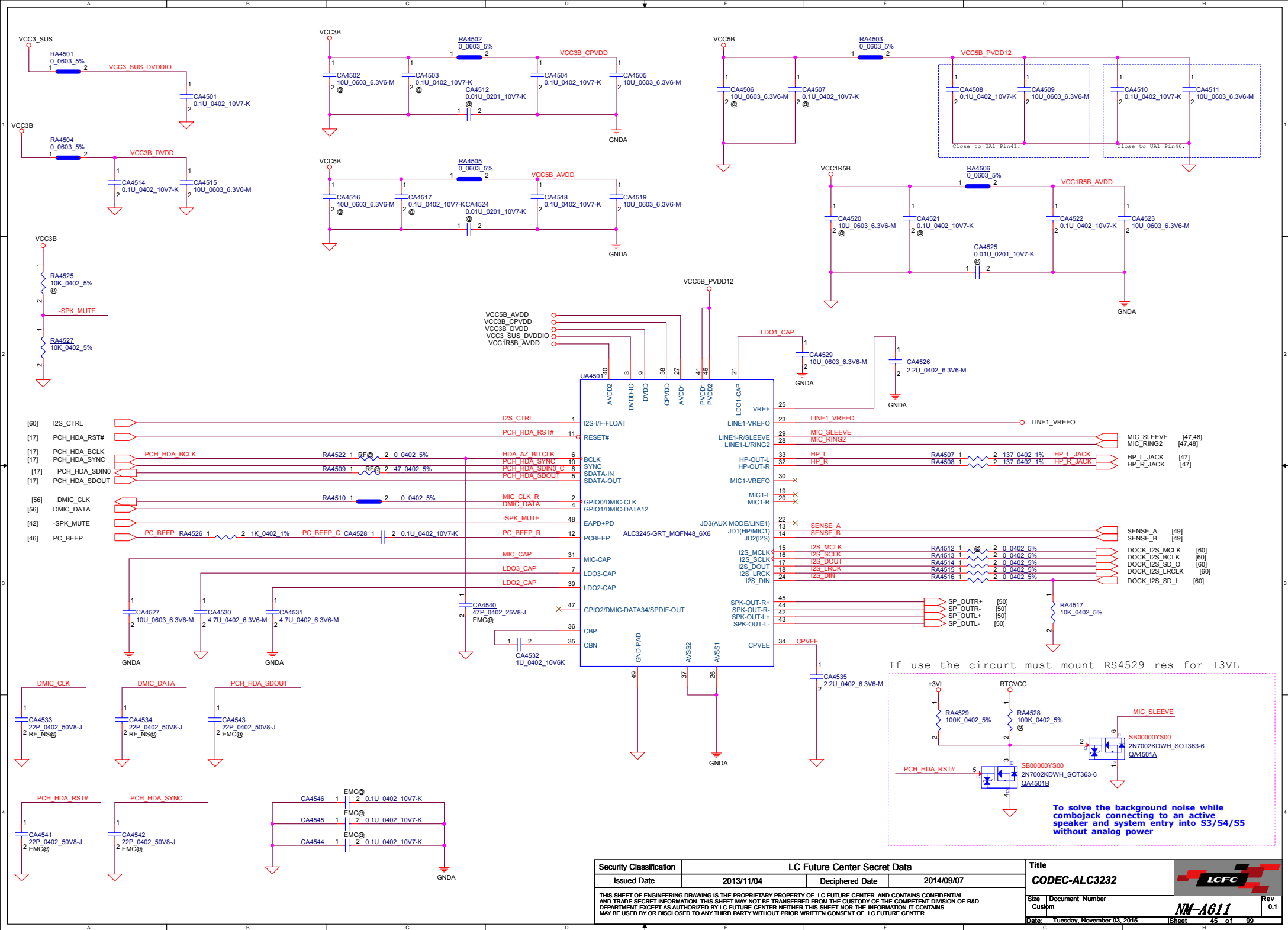
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Size	Document Number	Rev	
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Date:	Tuesday, November 03, 2015	Sheet	41 of 99





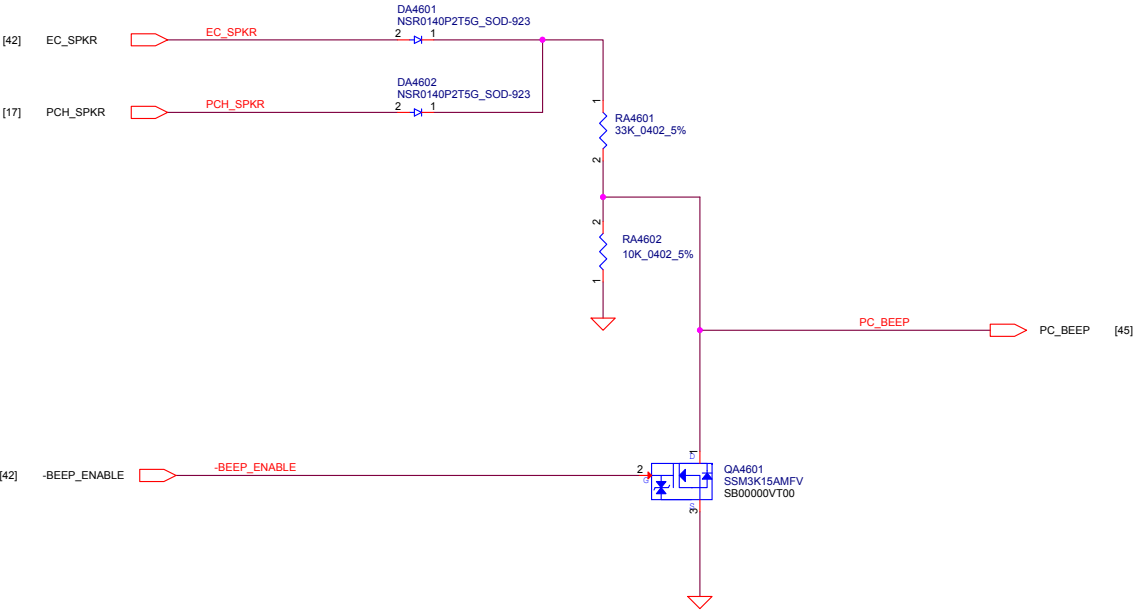


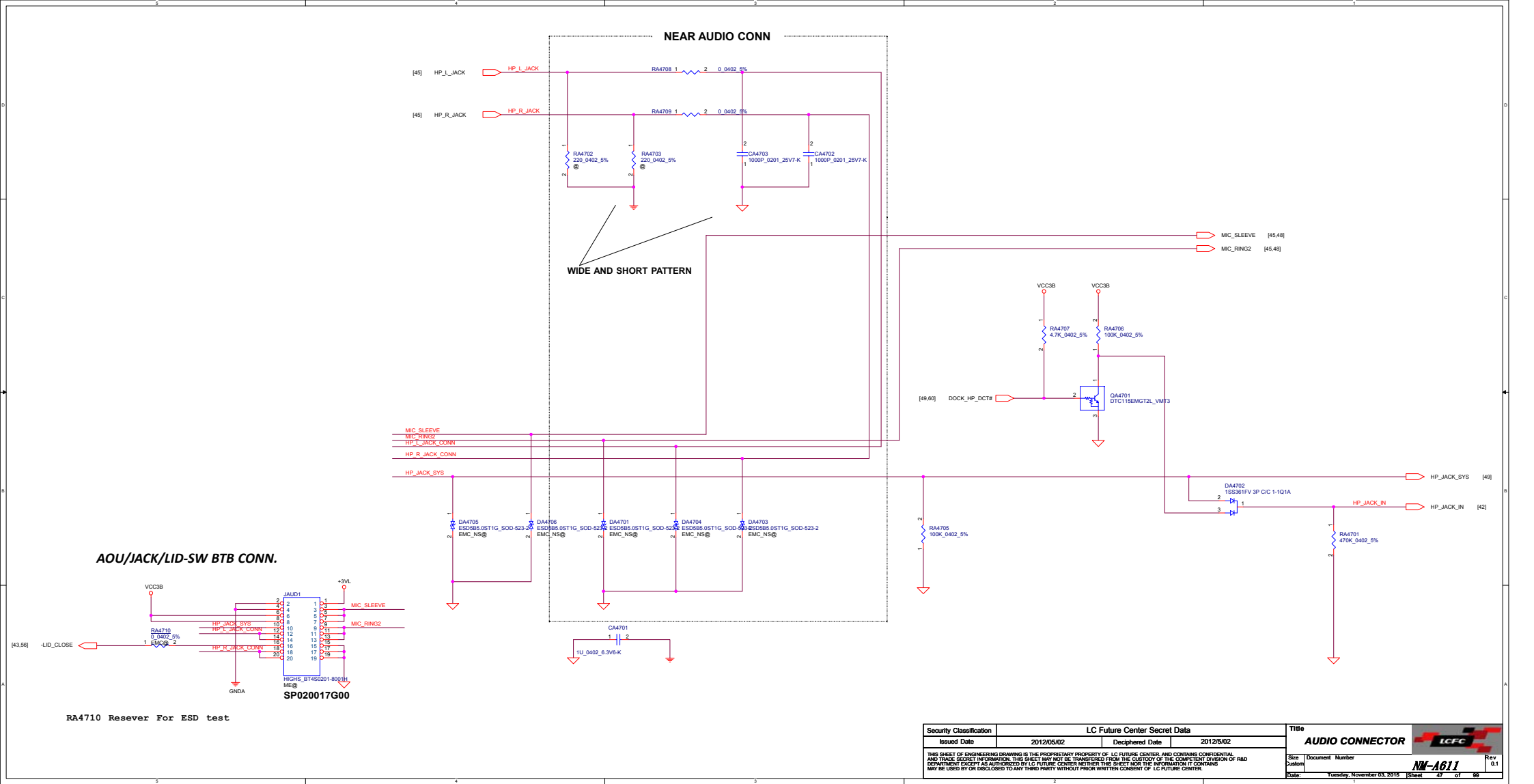


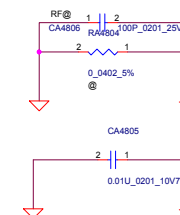
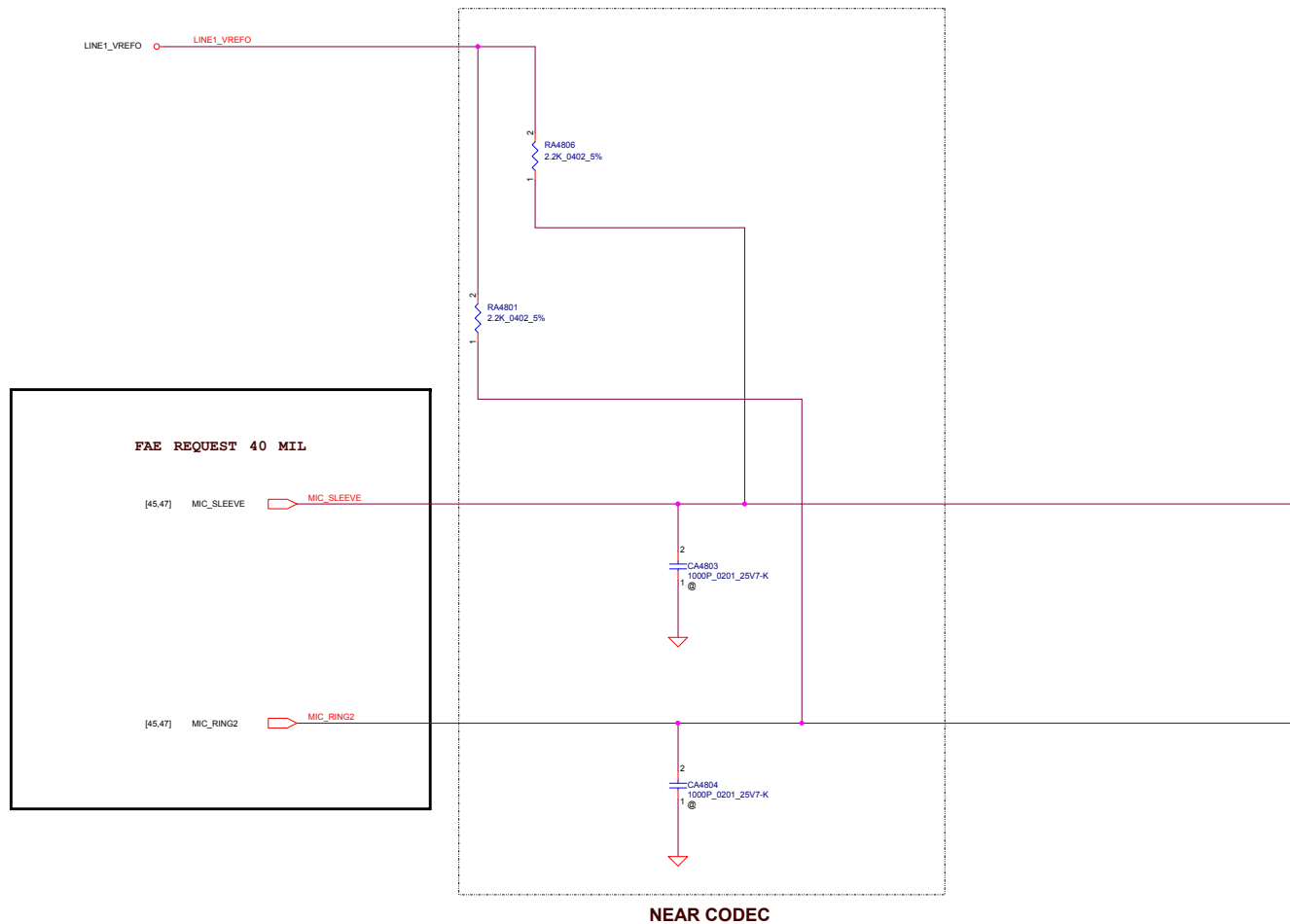


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PC-BEEP



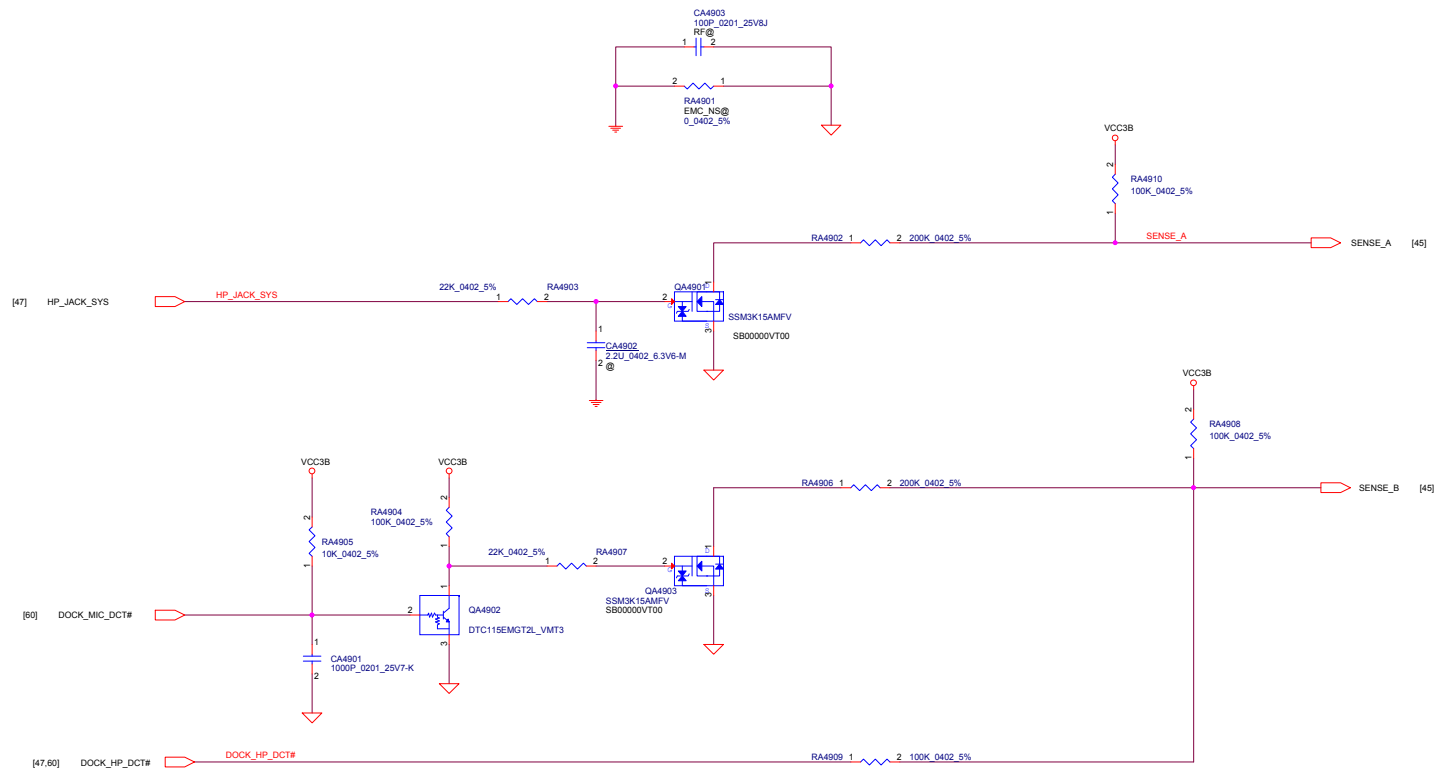




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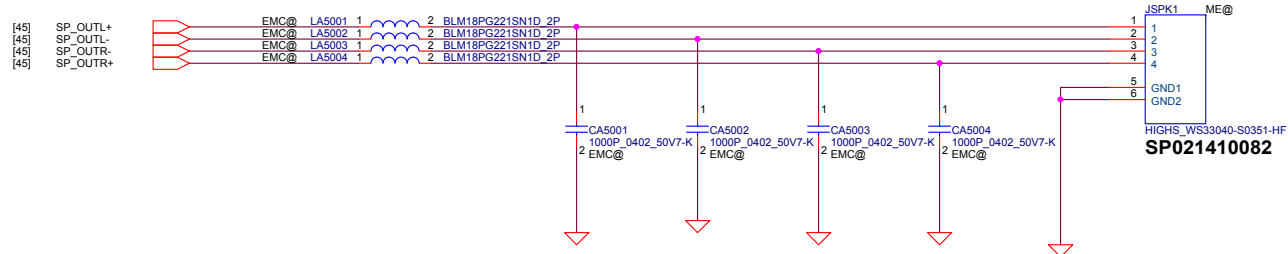
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				Rev	0.1



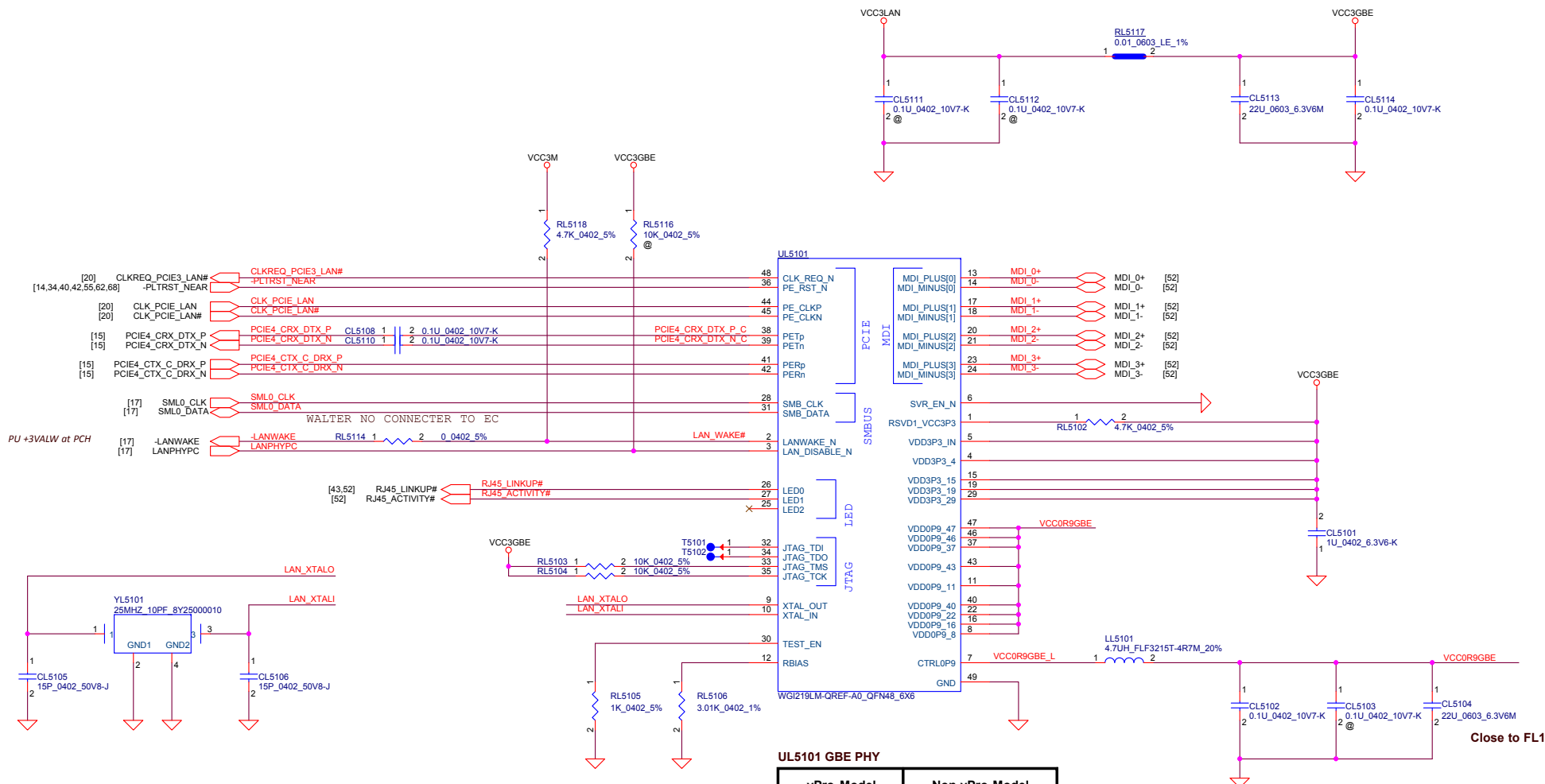
SPEAKER CONN.



PLACE, NEAR SPEAKER CONNECTOR

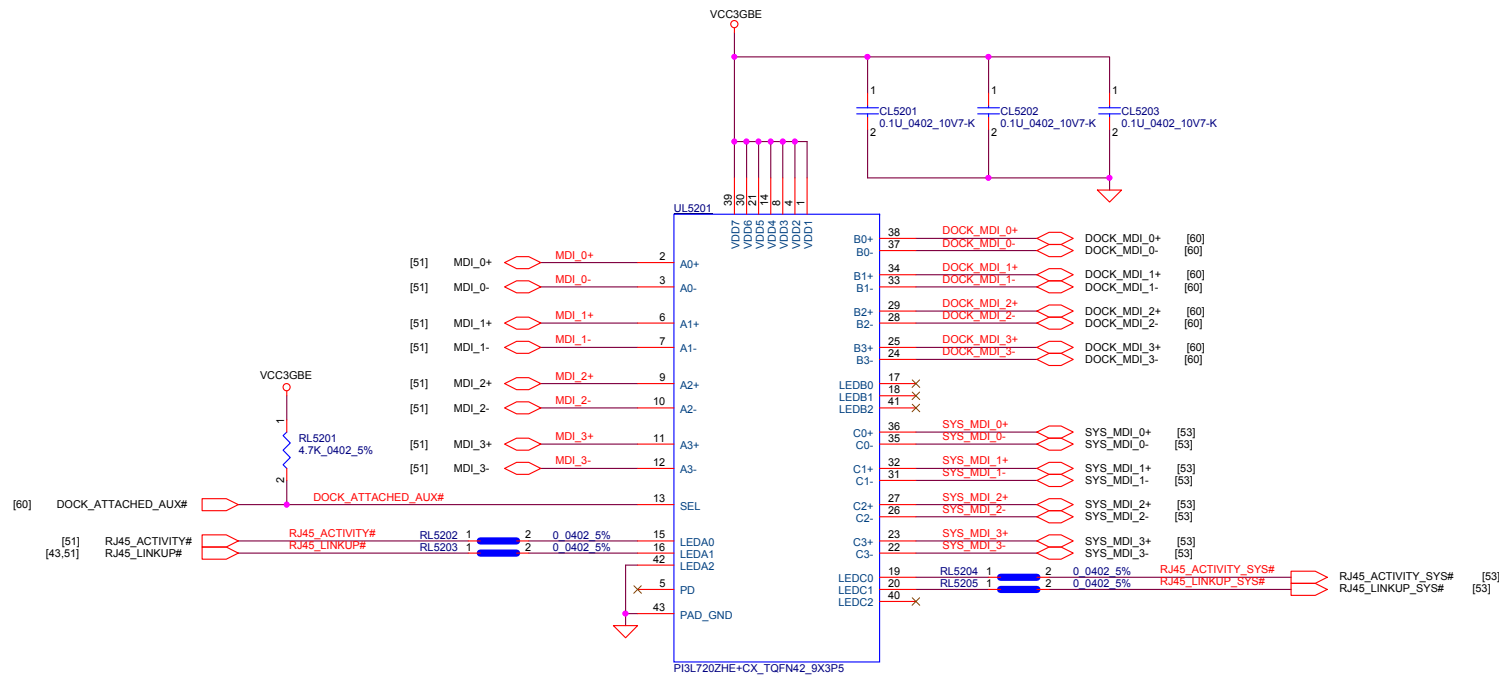
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				Rev	0.1





UL5101 GBE PHY

vPro Model	Non-vPro Model
WG1219LM	WG1219V
SA000073000	SA000072Z00



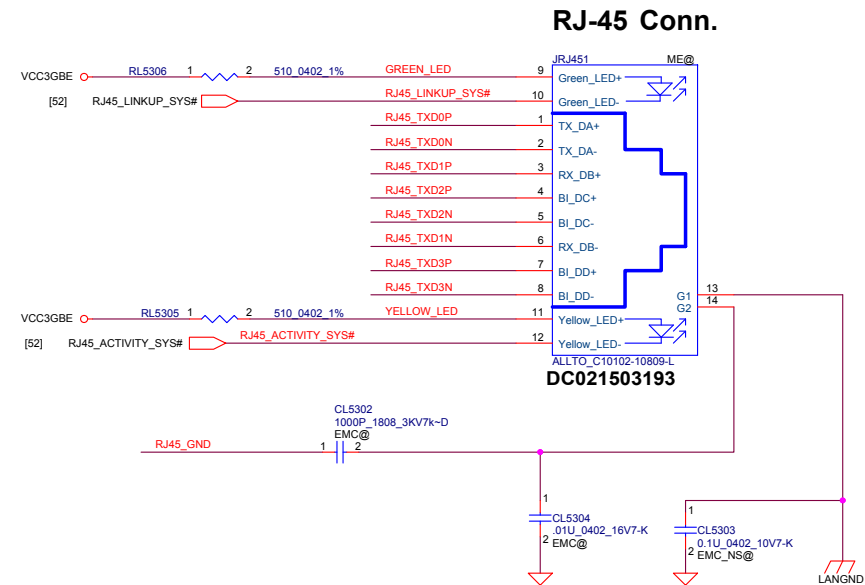
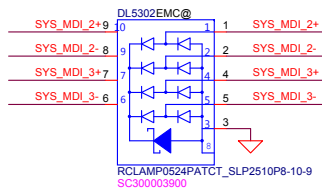
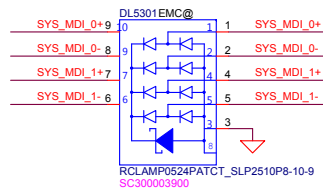
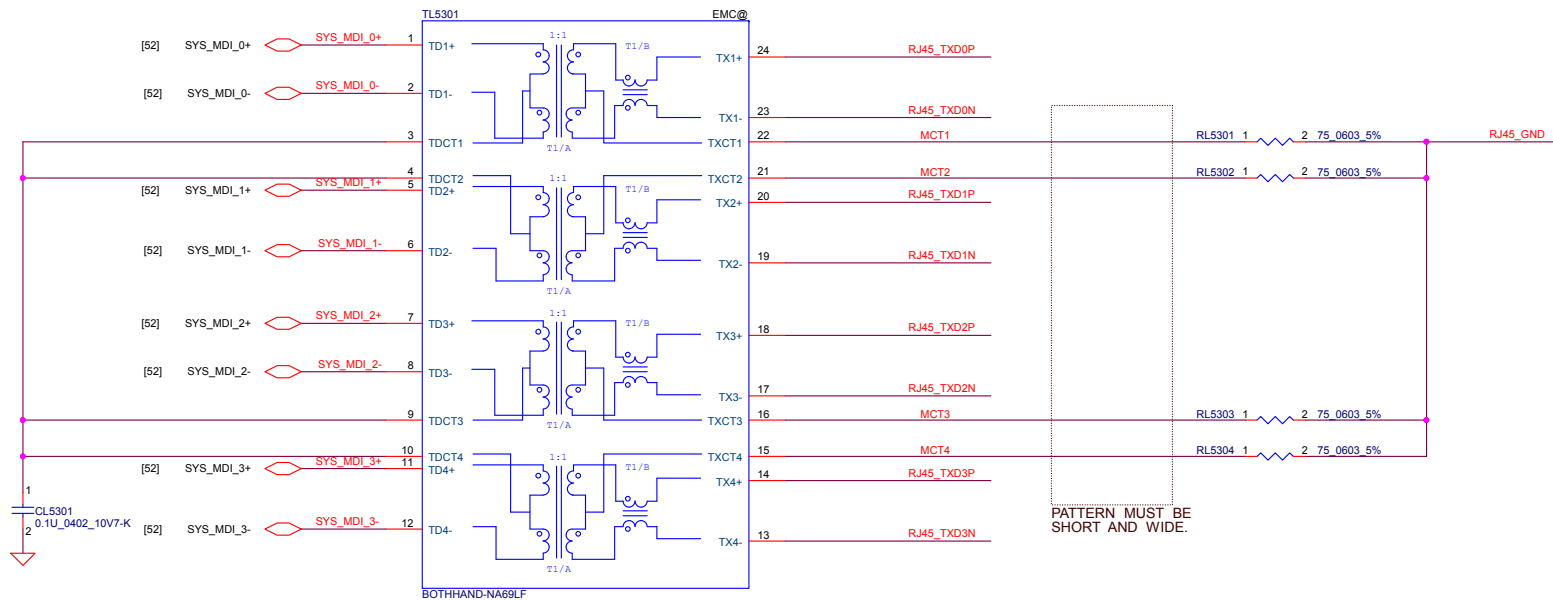
UL5201


Vendor	P/N	NOTE
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ONsemi	NCN7201, SA00005TF00	2nd Source (FVT)

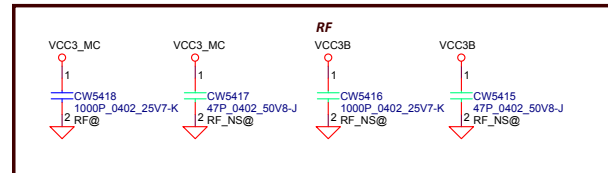
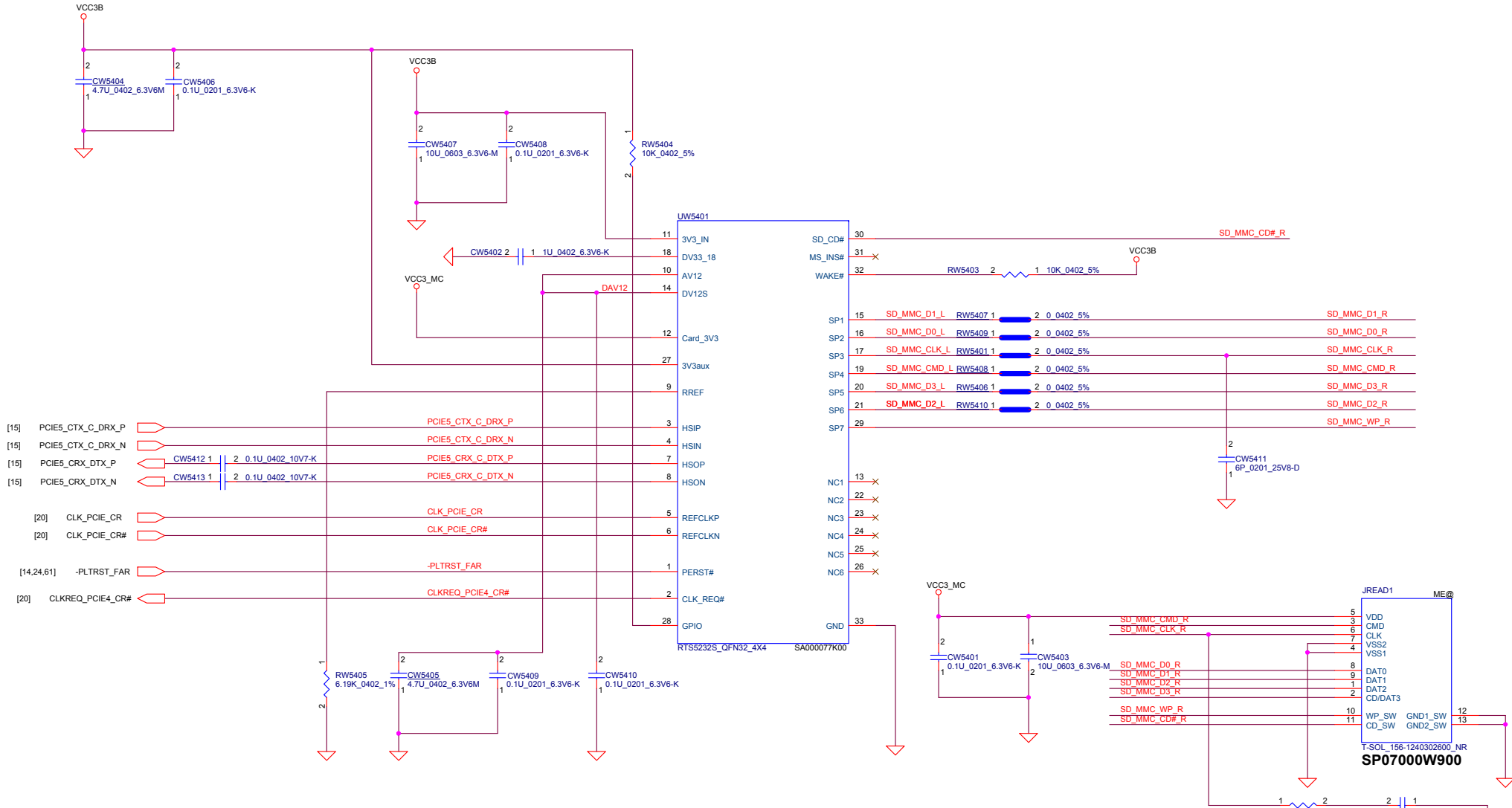
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GBE LAN SWITCH		0.1	
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Custom		NW-A611								0.1	
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APS G-Sensor

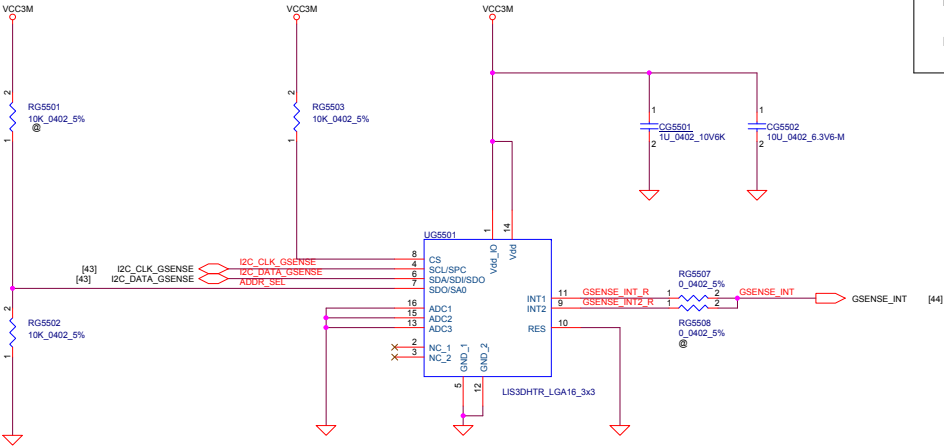
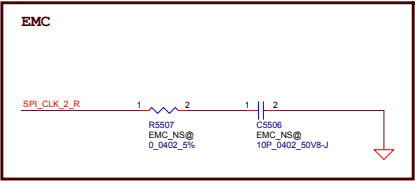
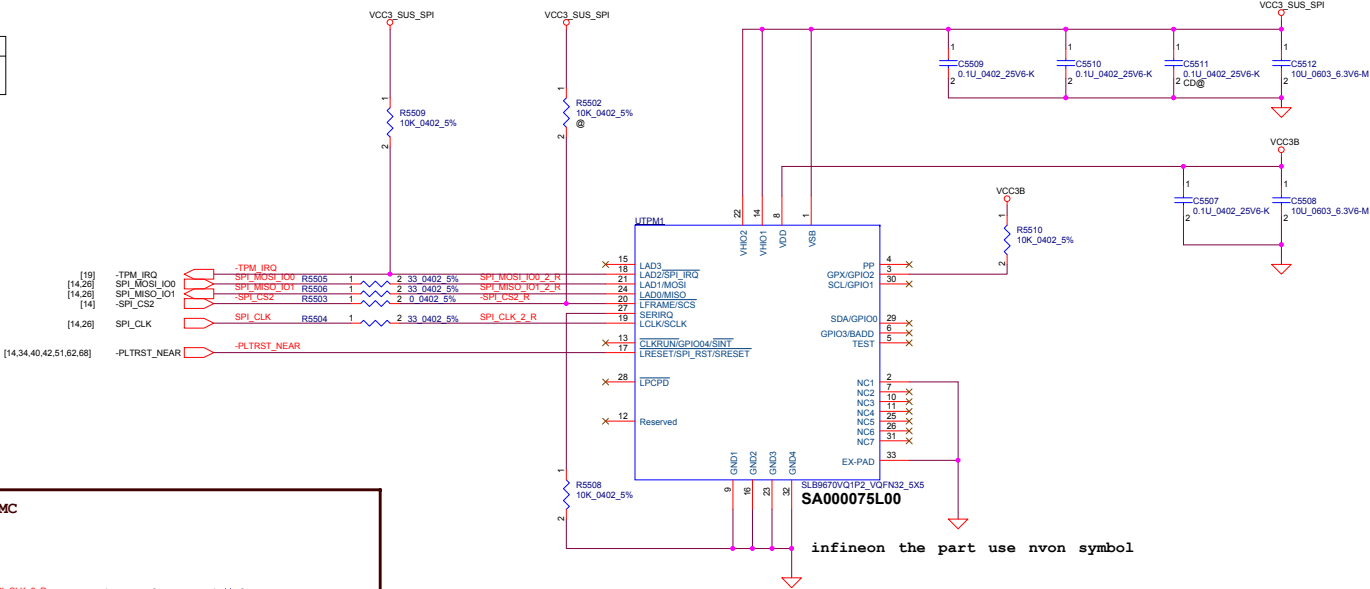


TABLE	
CS	Mode Selection
H	I2C Mode
L	SPI Mode

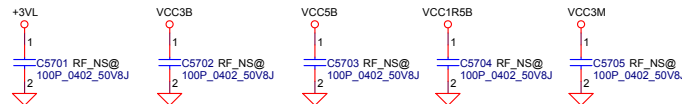
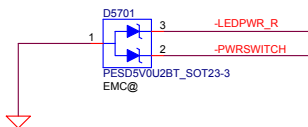
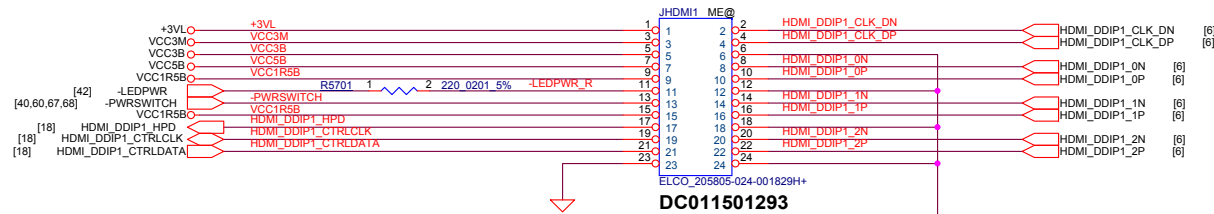
TPM IC

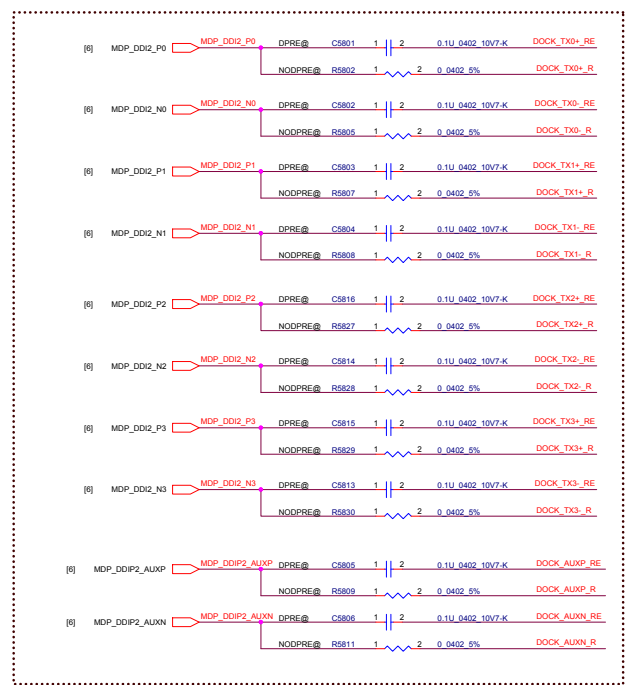
TPM Pin8	+3VS	VCC3_SUS_SPI
S3~S5 current	120uA	330uA



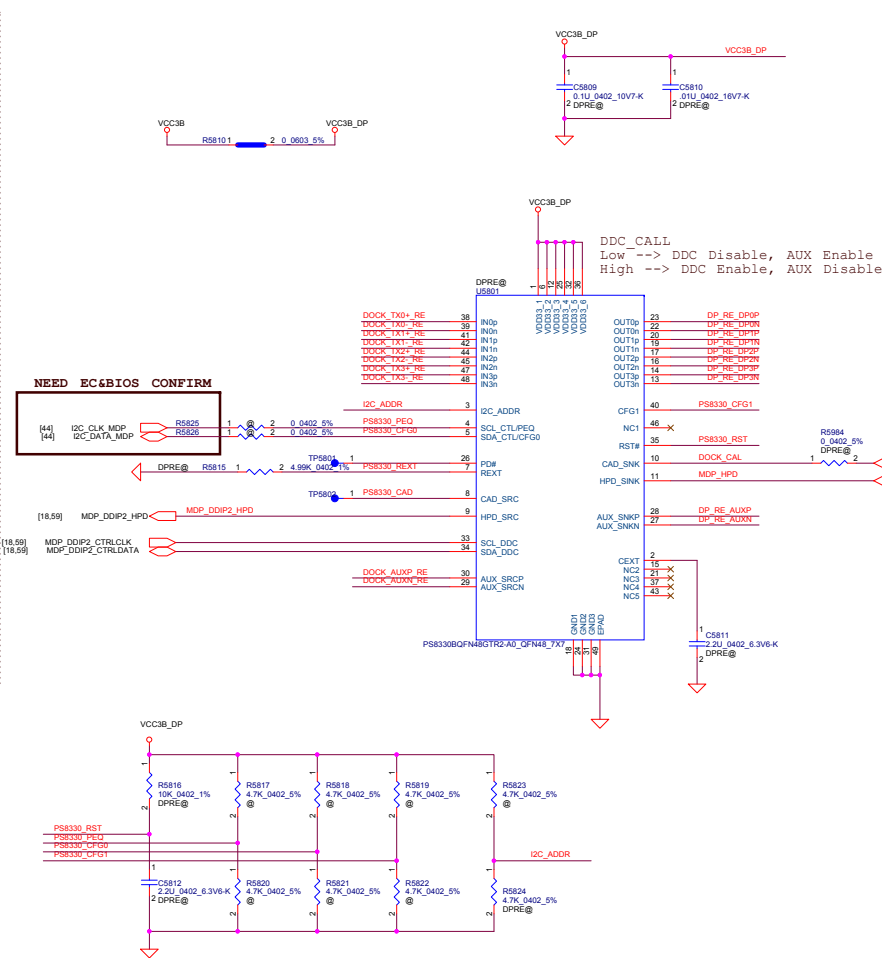
infineon the part use nvon symbol

M/B TO HDMI/B BTB CONN.

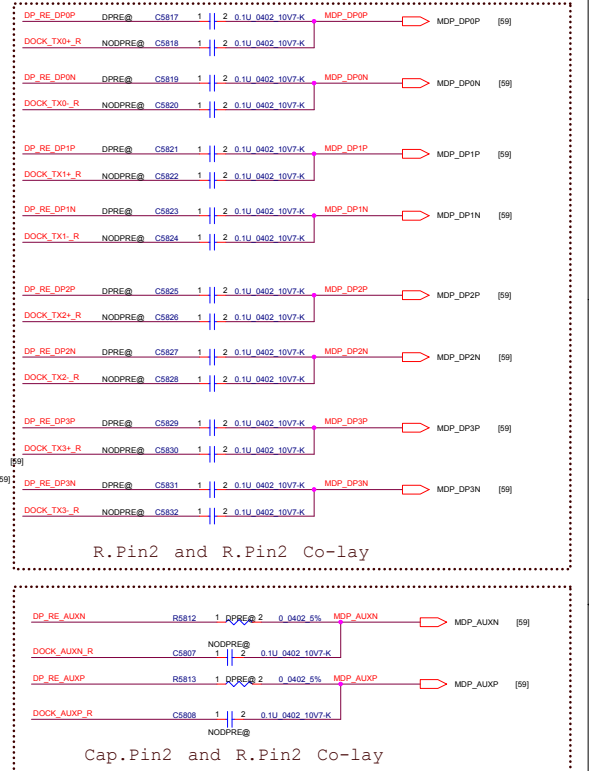




Cap.Pin1 and R.Pin1 Co-lay



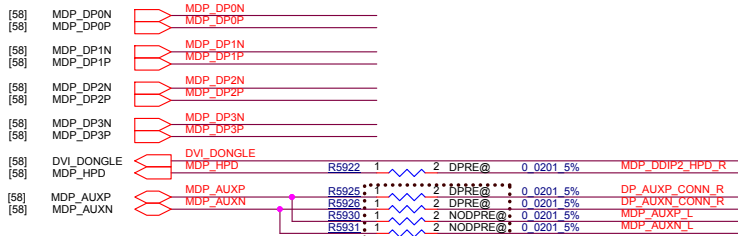
NEED EC&BIOS CONFIRM



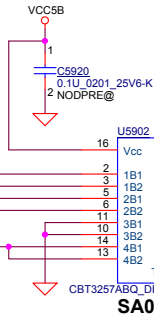
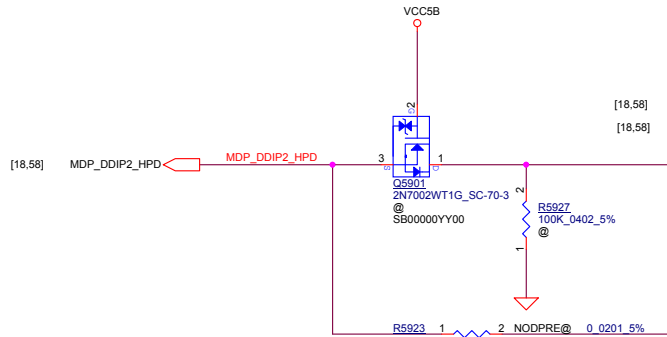
R.Pin2 and R.Pin2 Co-lay

Cap.Pin2 and R.Pin2 Co-lay

DP AUX : From Repeater don't need cap, but PCH.

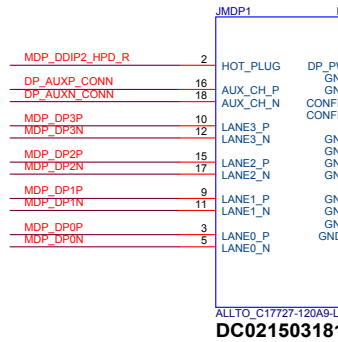


PIN1 COLAY

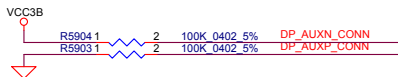


PIN2 COLAY

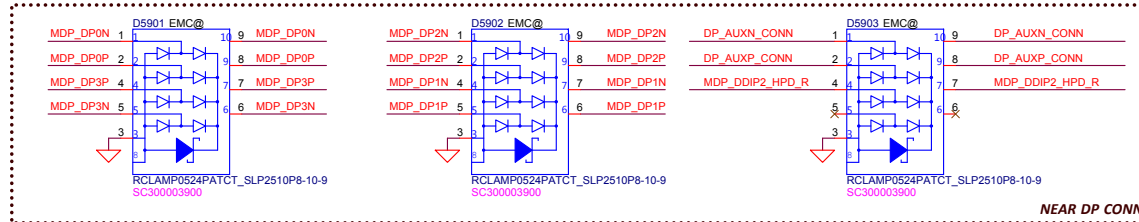
OE	S	Result
L	L	nA1 to nB1.
L	H	nA1 to nB2.
H	X	Switch off.



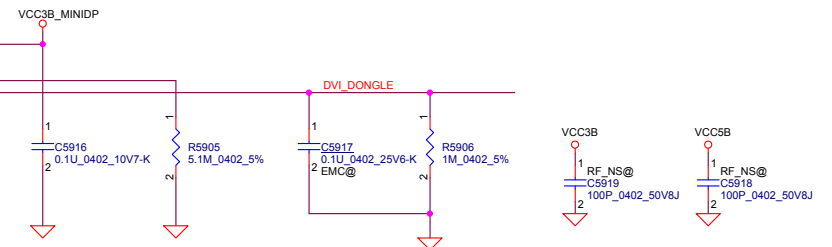
DC021503181



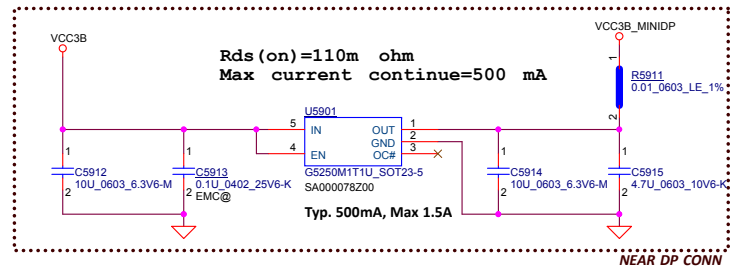
EMC (ESD soluti on)



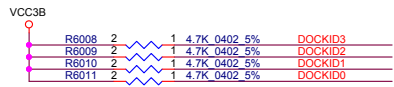
NEAR DP CONN



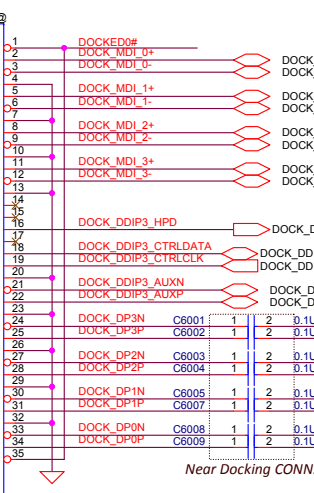
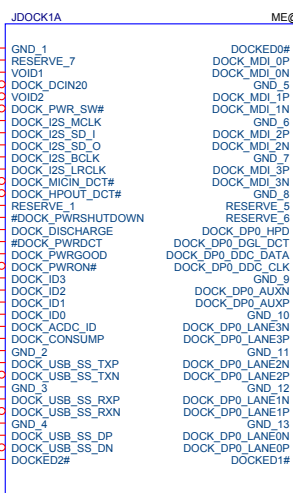
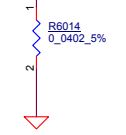
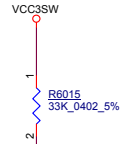
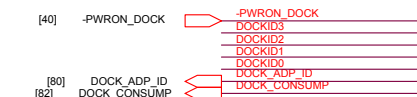
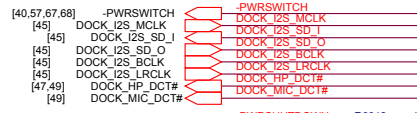
Rds(on)=110m ohm
Max current continue=500 mA



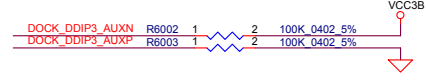
NEAR DP CONN



[14] DOCKID[3:0]

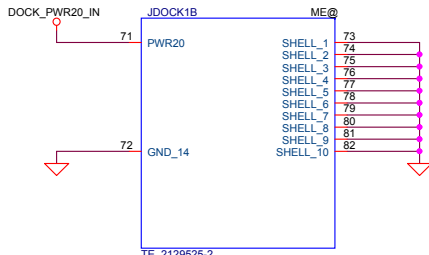
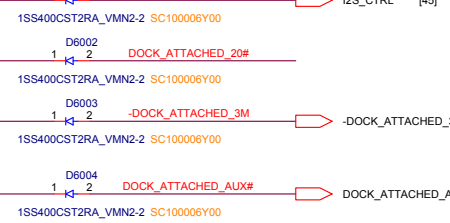


Near Docking CONN.



TE_2129525-2

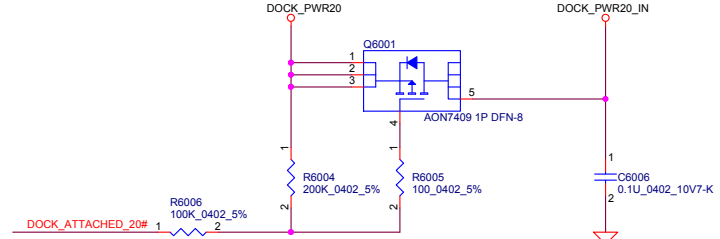
SP030000Z00



TE_2129525-2

SP030000Z00

Rds(on)=11.5m ohm
Max current continue=6.75A(Adapter 135W)

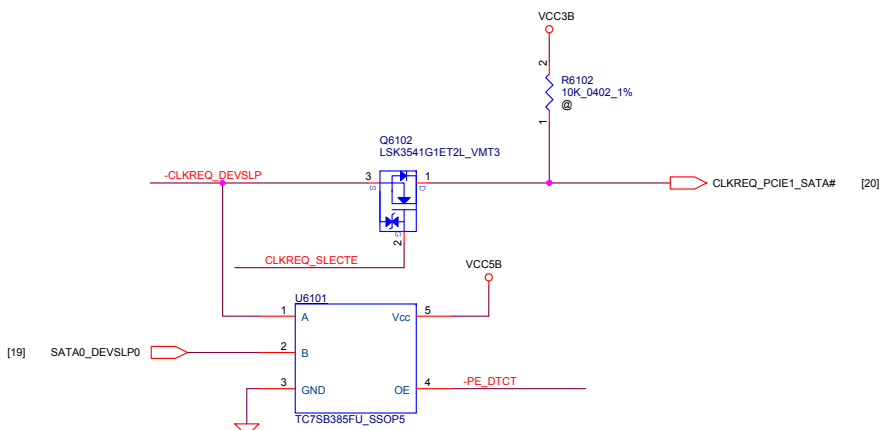
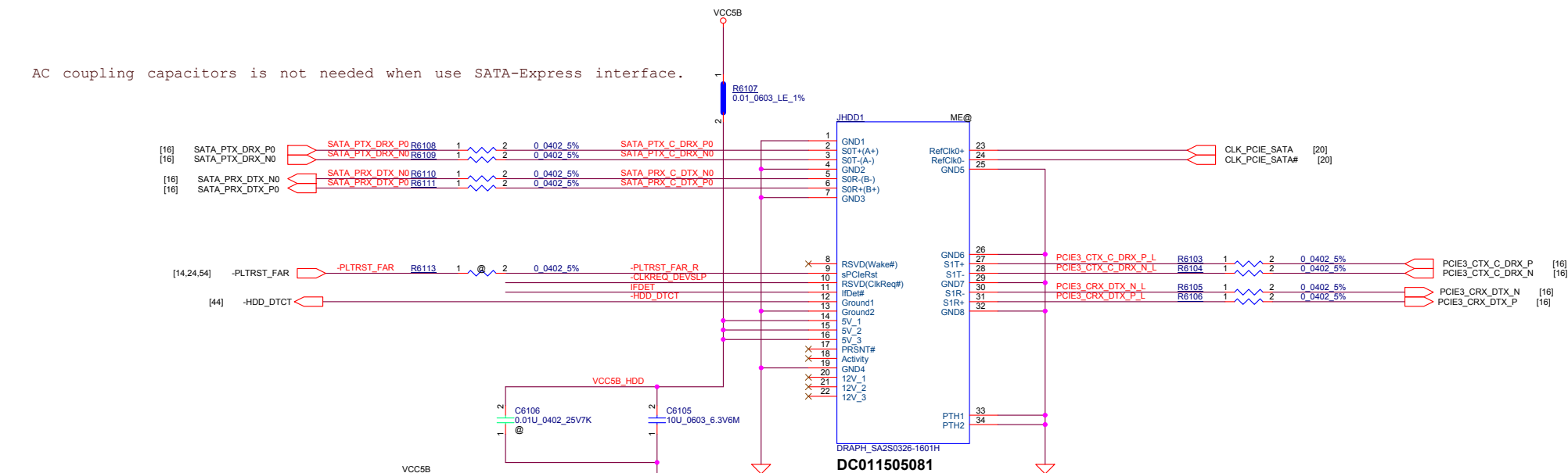


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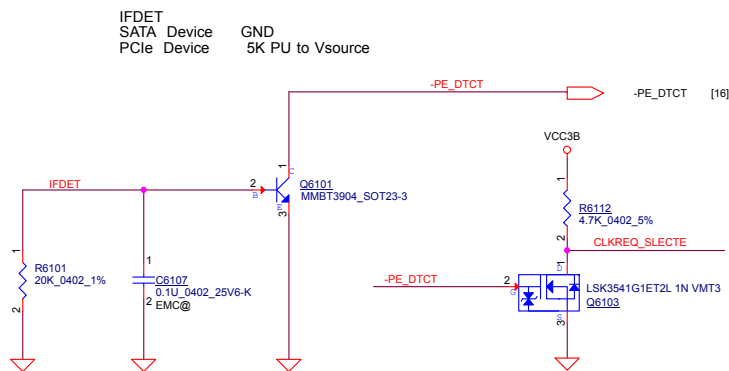
Title		Rev	
DOCKING CONN.		0.1	
Size	Document Number	NM-A611	
Date	Tuesday, November 03, 2015	Sheet	60 of 99

WWW.AliSaler.Com

AC coupling capacitors is not needed when use SATA-Express interface.



Input	Function
OE	
L	Disconnect
H	A port = B port

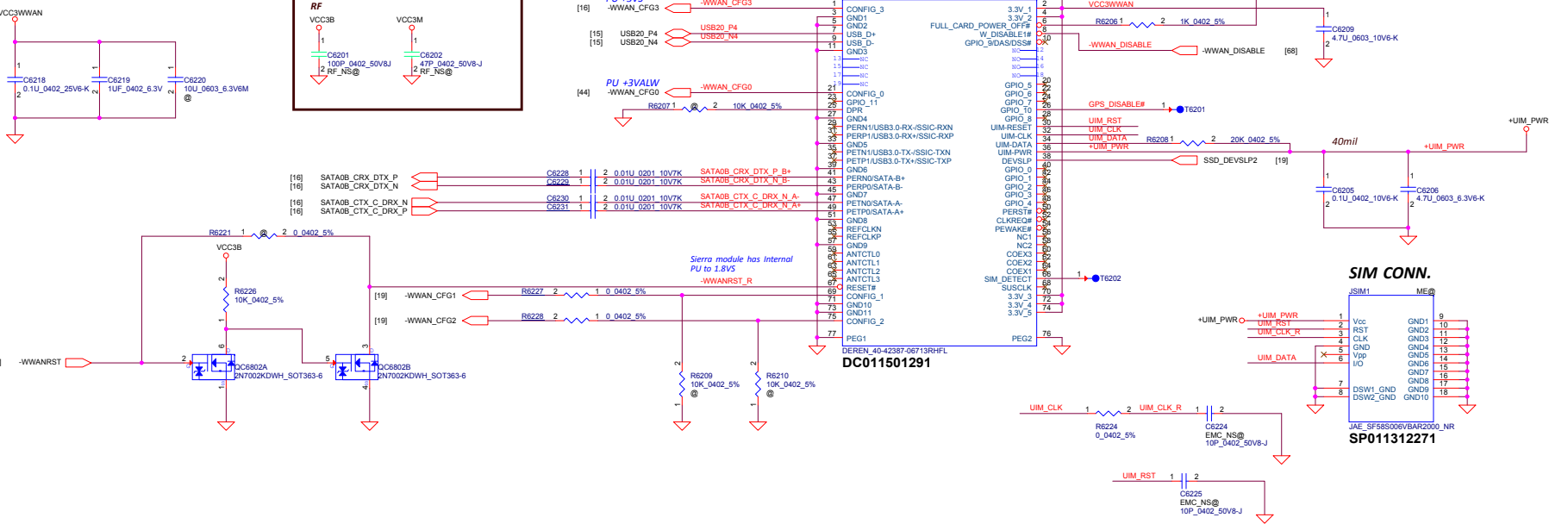


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Issued Date	2013/11/04	Deciphered Date
		2014/09/07

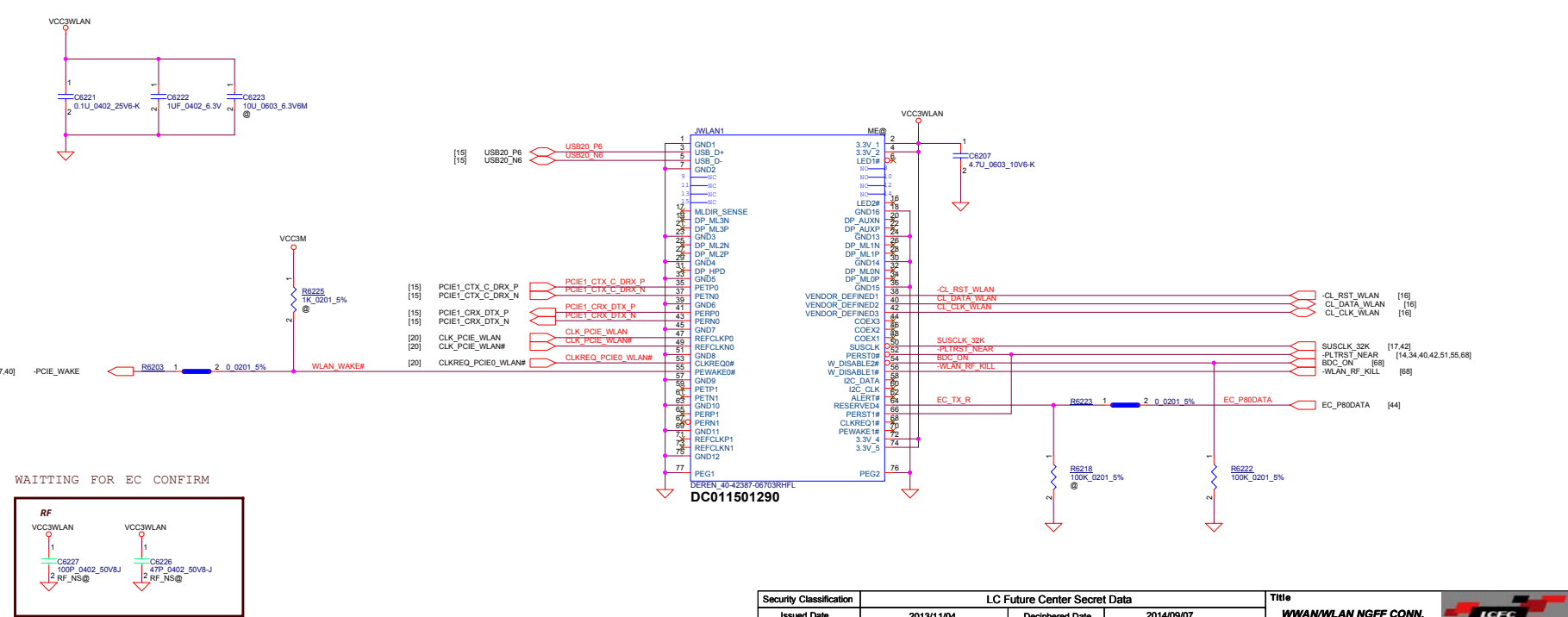
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Title		SATA HDD CONN.	
Size	Document Number	Rev	0.1
Custom			
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TYPE-B NGFF SLOT FOR WWAN/SSD
3.2H CONNECTOR

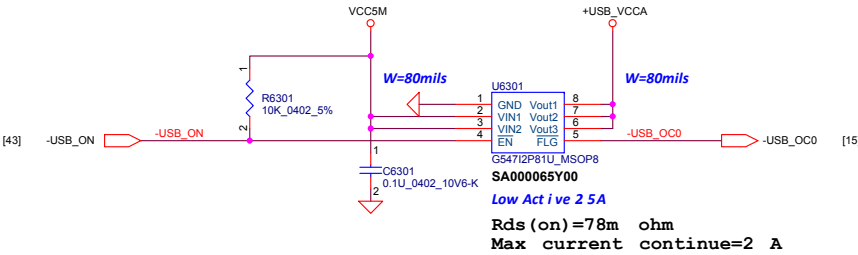


TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR

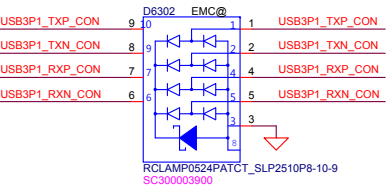
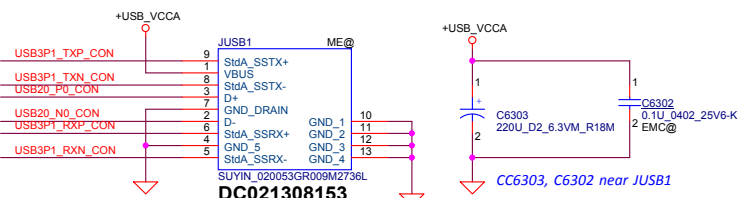
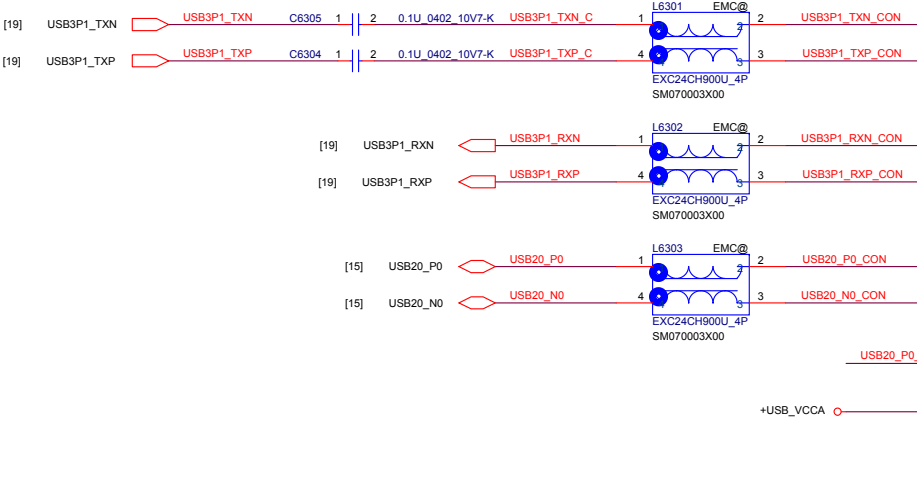


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2013/1/04		2014/09/07			
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Size		Document Number			
Custom		NM-A611		Sheet 02 of 09	
Date:		Tuesday, November 03, 2015			

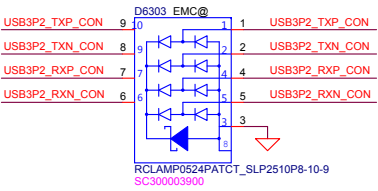
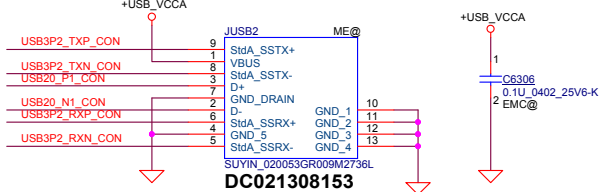
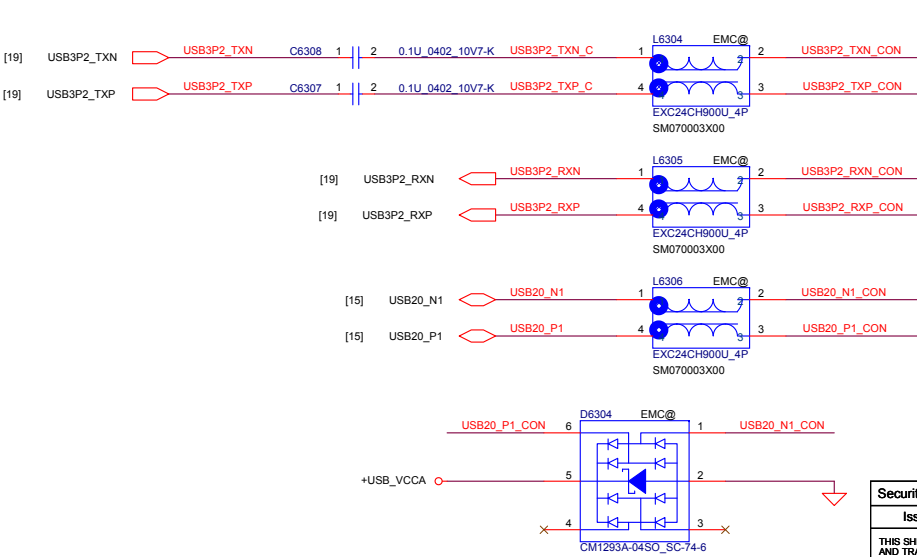
USB POWER SWITCH



On Board (Right-Front)



On Board (Right-Back)



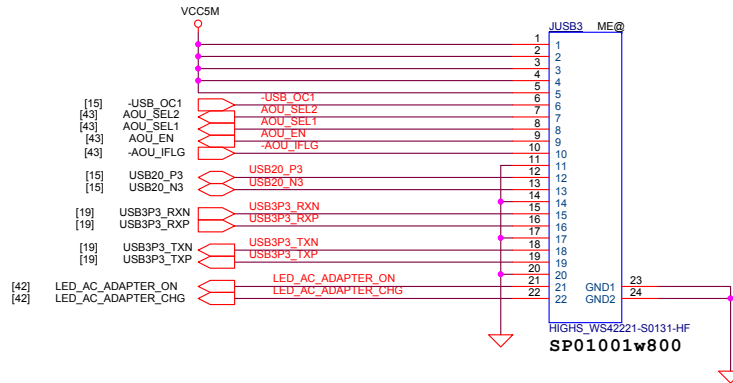
*


MB PIN number	MB PIN name	SB board pin name	SB PIN number
pin1~5	VCC5M	VCC5M	pin1~5
pin6	-USB_OC1	-USB_OC1	pin6
pin7	AOU_SEL2	AOU_SEL2	pin7
pin8	AOU_SEL1	AOU_SEL1	pin8
pin9	AOU_EN	AOU_EN	pin9
pin10	-AOU_IFLG	-AOU_IFLG	pin10
pin11	GND	GND	pin11
pin12	USB20_P3	USB20_P3	pin12
pin13	USB20_N3	USB20_N3	pin13
pin14	GND	GND	pin14
pin15	USB3P3_RXN	USB3P3_RXN	pin19
pin16	USB3P3_RXP	USB3P3_RXP	pin18
pin17	GND	GND	pin17
pin18	USB3P3_TXN	USB3P3_TXN	pin16
pin19	USB3P3_TXP	USB3P3_TXP	pin15
pin20	GND	GND	pin20
pin21	LED_AC_ADAPTER_ON	LED_AC_ADAPTER_ON	pin21
pin22	LED_AC_ADAPTER_CHG	LED_AC_ADAPTER_CHG	pin22

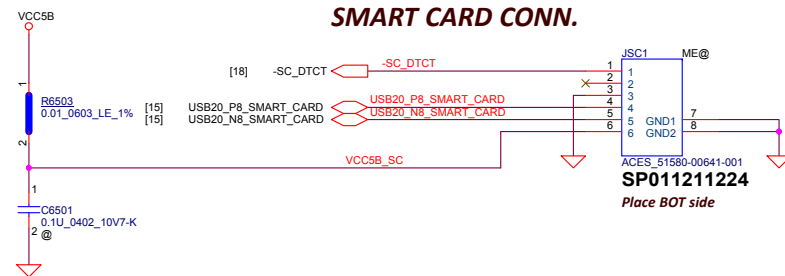
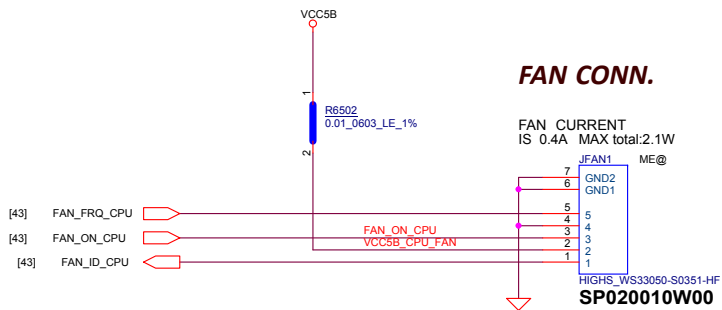
*

USB board and MB board is wire to board connector.
Due to USB board layout issue so pin define can* meet MB

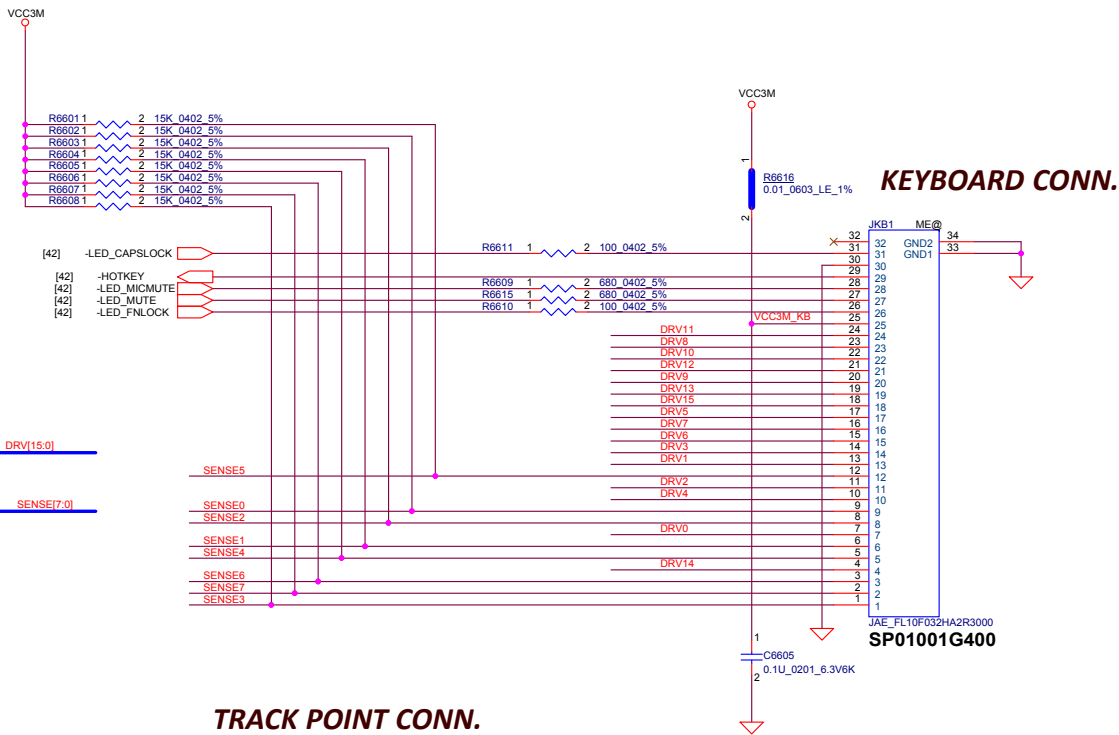
USB LEFT PORT



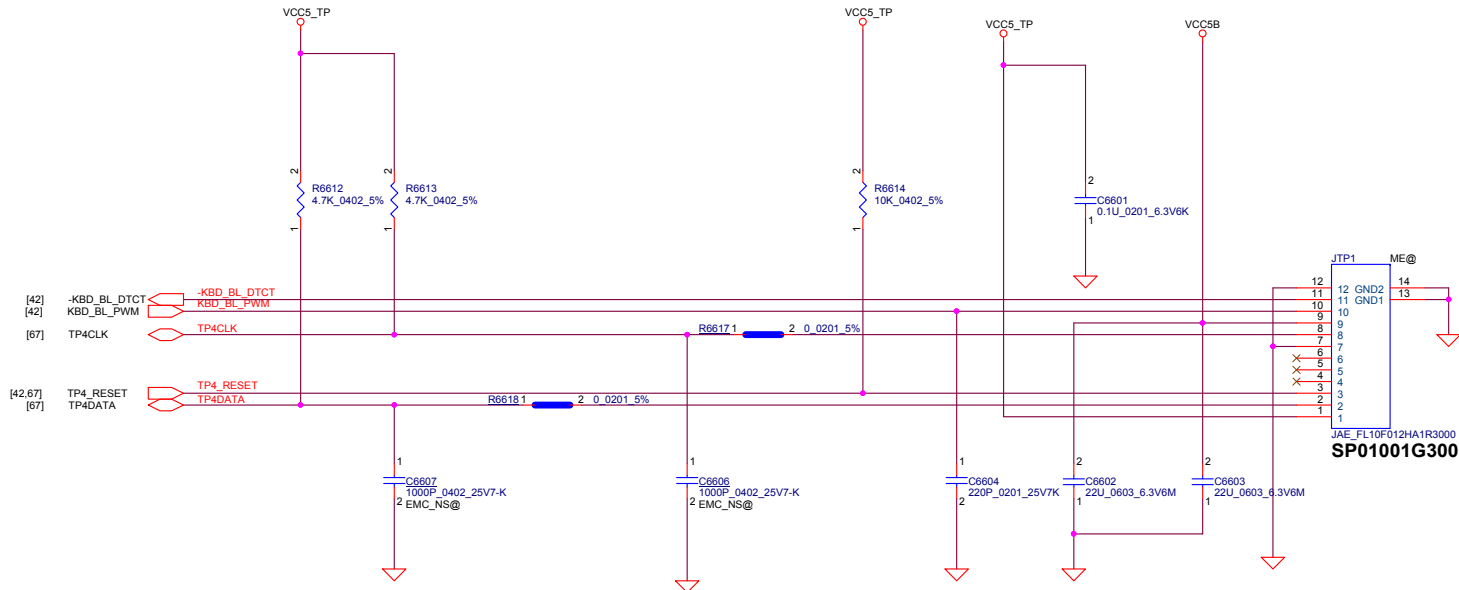
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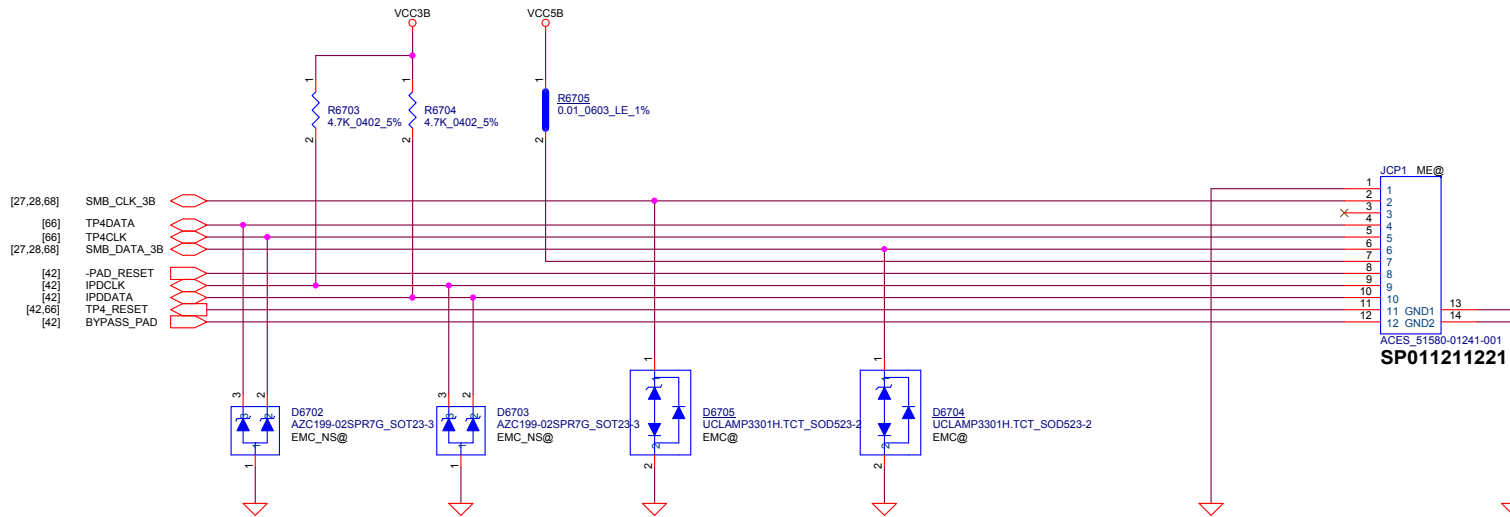
TRACK POINT CONN.



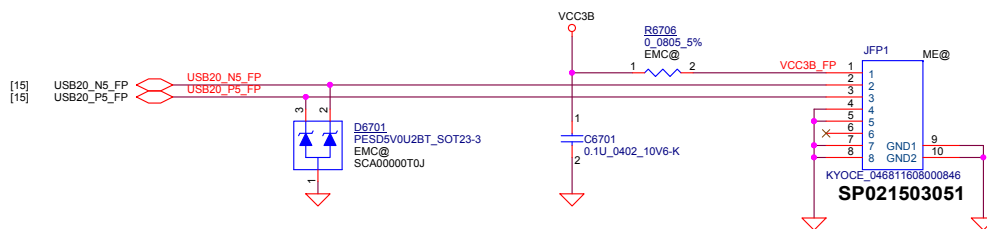
Security Classification		LC Future Center Secret Data		Title	
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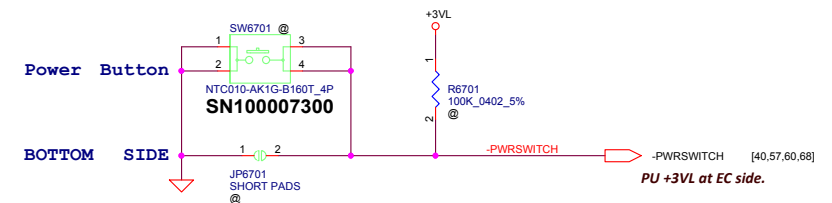
Click Pad



FingerPrint CONN.

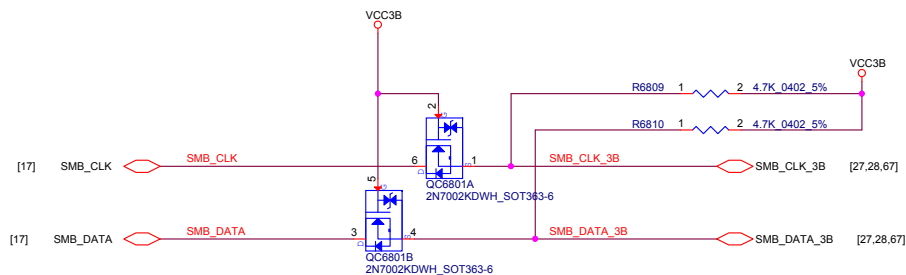
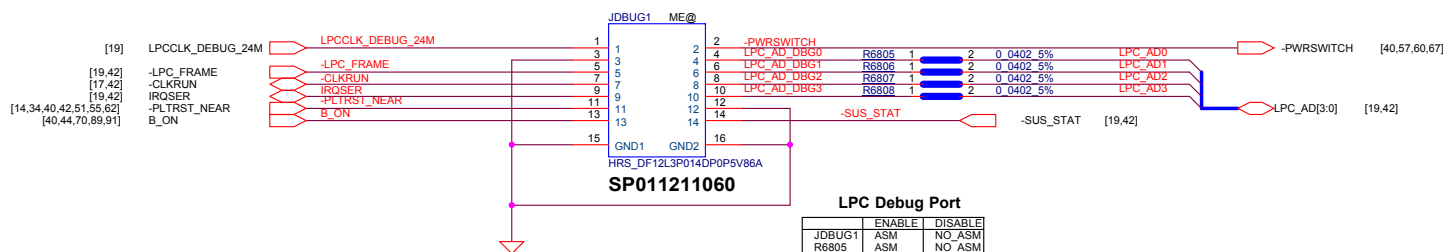
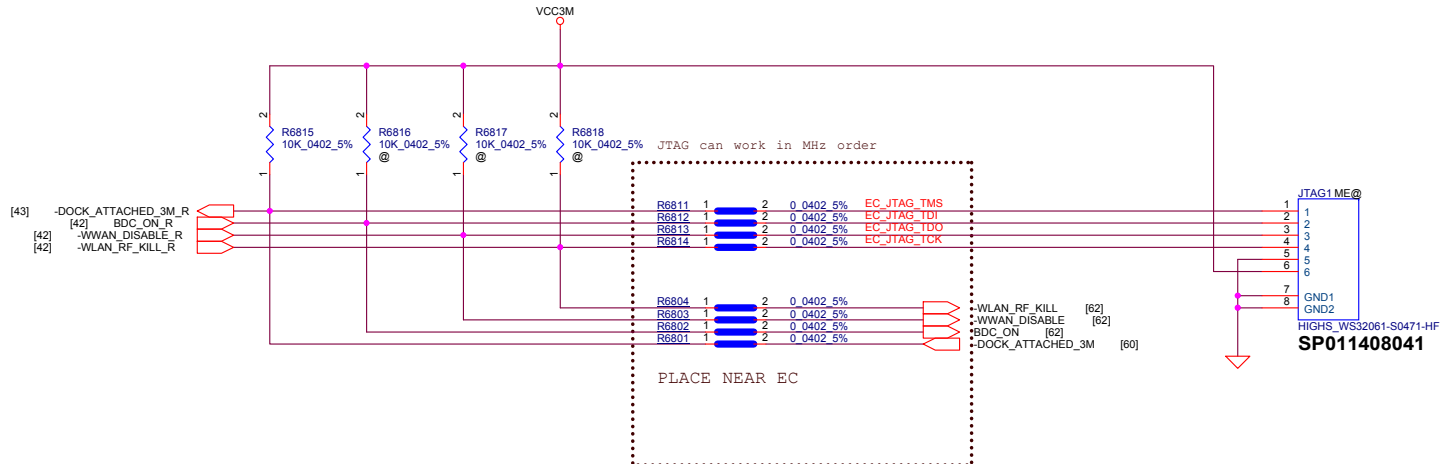


PWRBTN FOR DEBUG



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EMC

LPCCLK_DEBUG_24M R6819 1 2 0.0402 5% C6801 1 2 10P 0402 50V8-J

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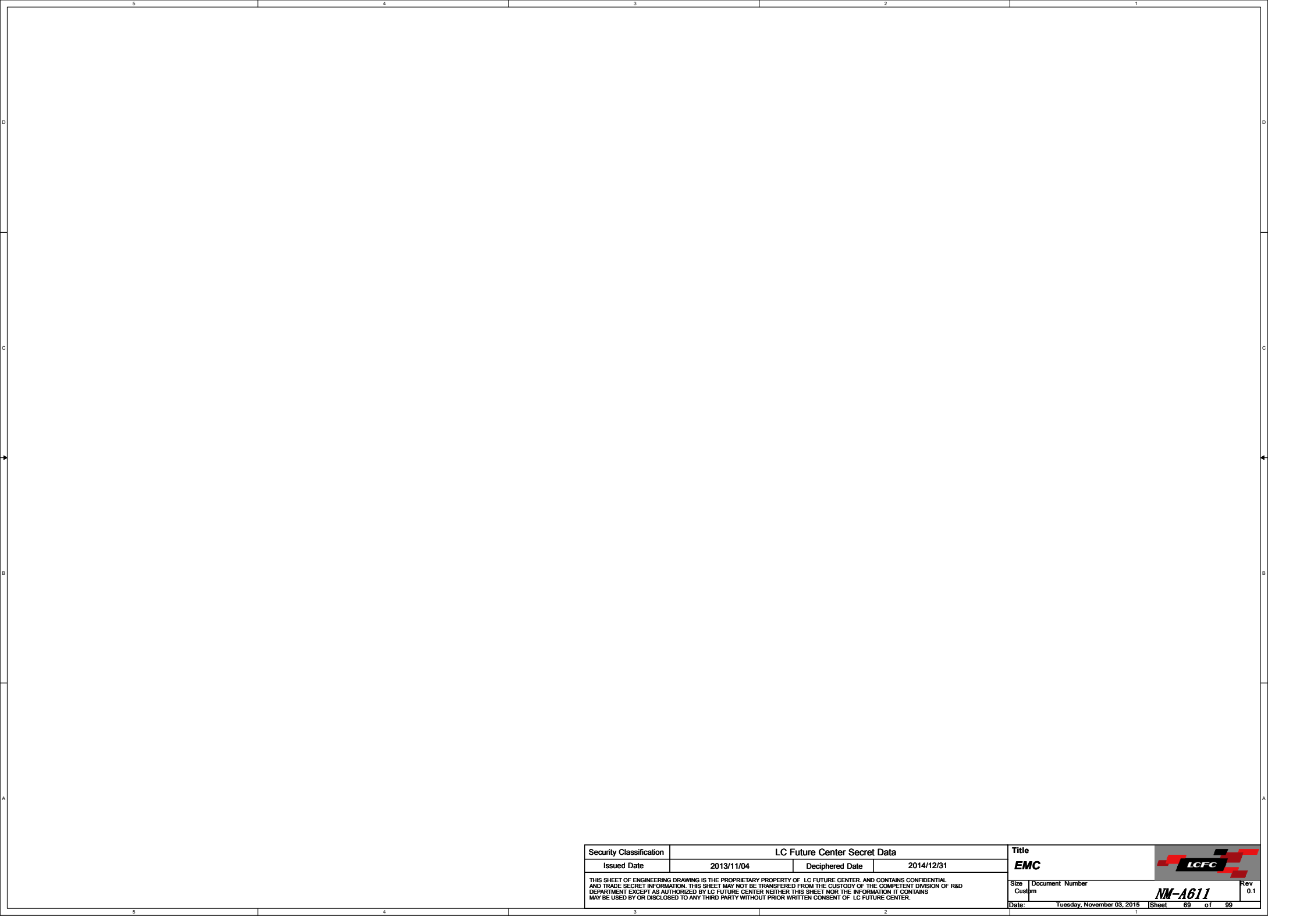
Title		SMBUS SWITCH/LPC DEBUG	
Size	Document Number	Rev	
Custom		0.1	
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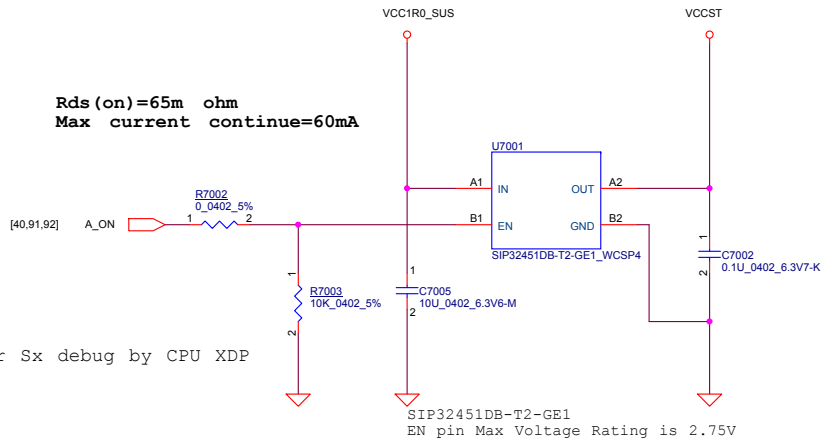
Rev

0.1

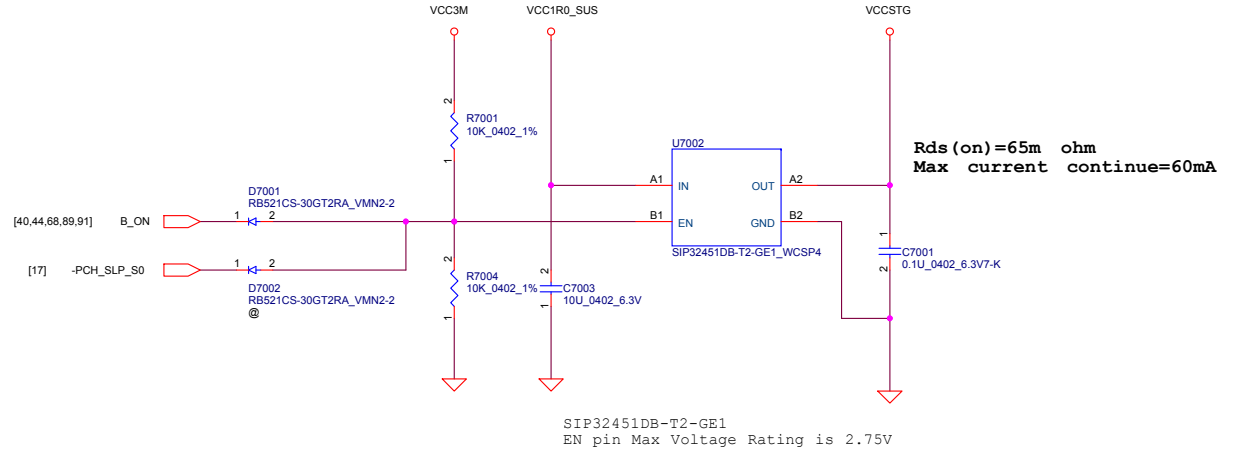
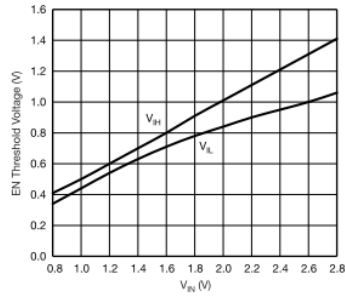


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					Custom	NM-A611	0.1
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Rds(on)=65m ohm
Max current continue=60mA



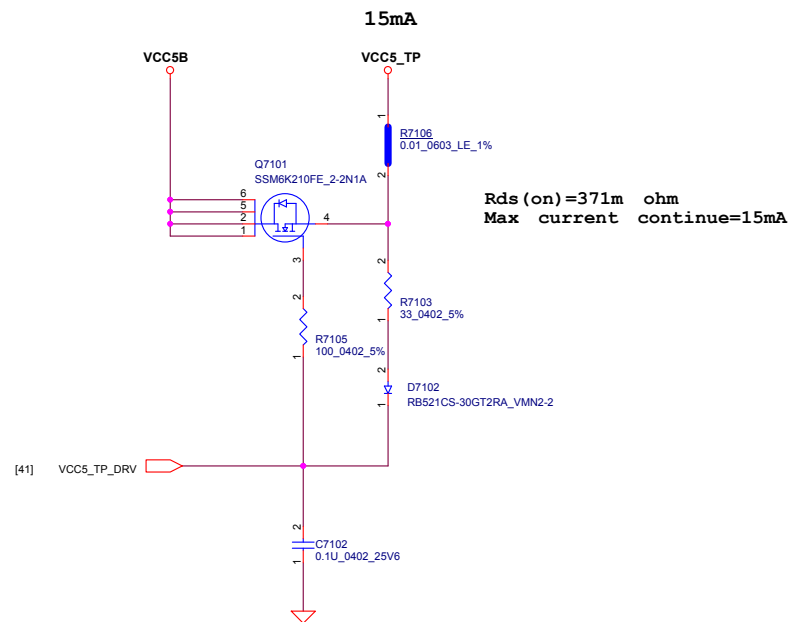
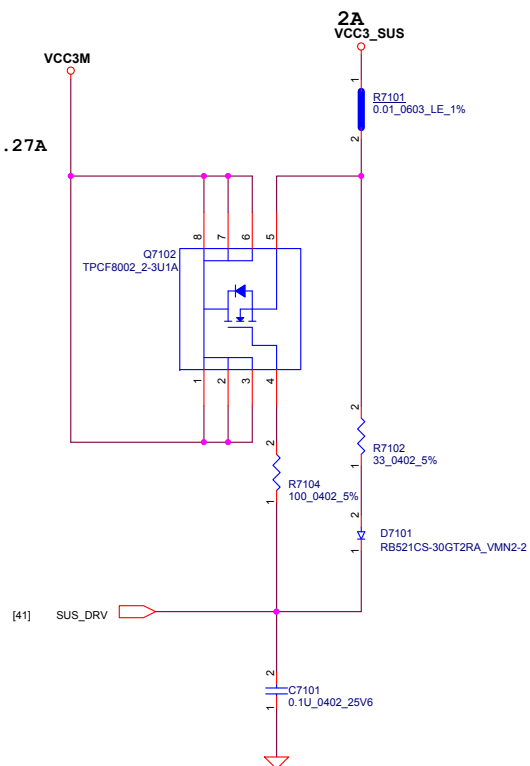
For Sx debug by CPU XDP



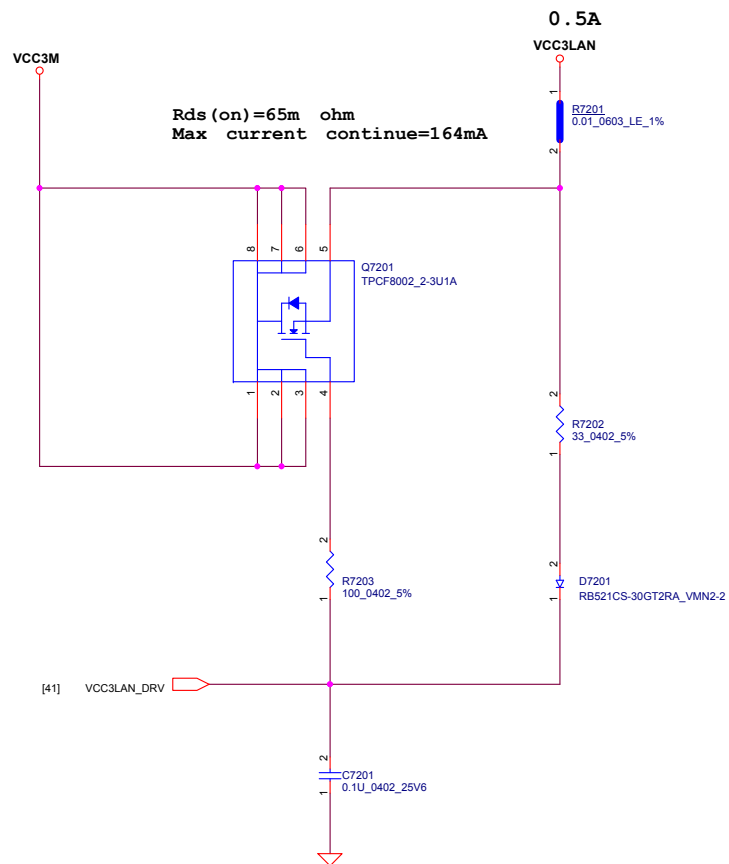
Rds(on)=65m ohm
Max current continue=60mA


Security Classification		LC Future Center Secret Data		Title		LOAD SW VCCST/VCCSTG		ICFC	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	Size	Document Number	Rev	0.1	NM-A611	
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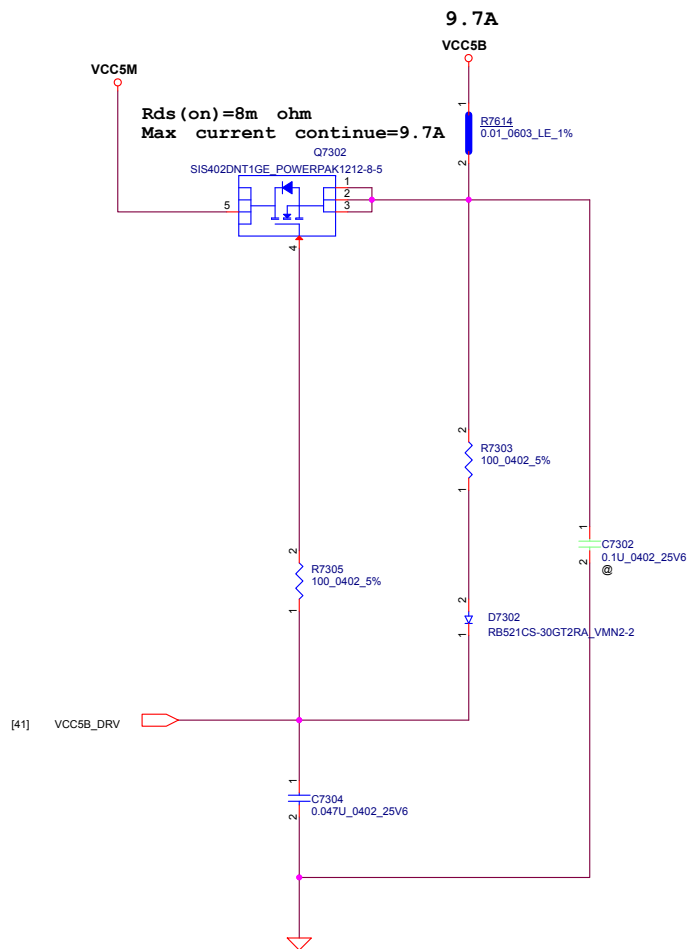
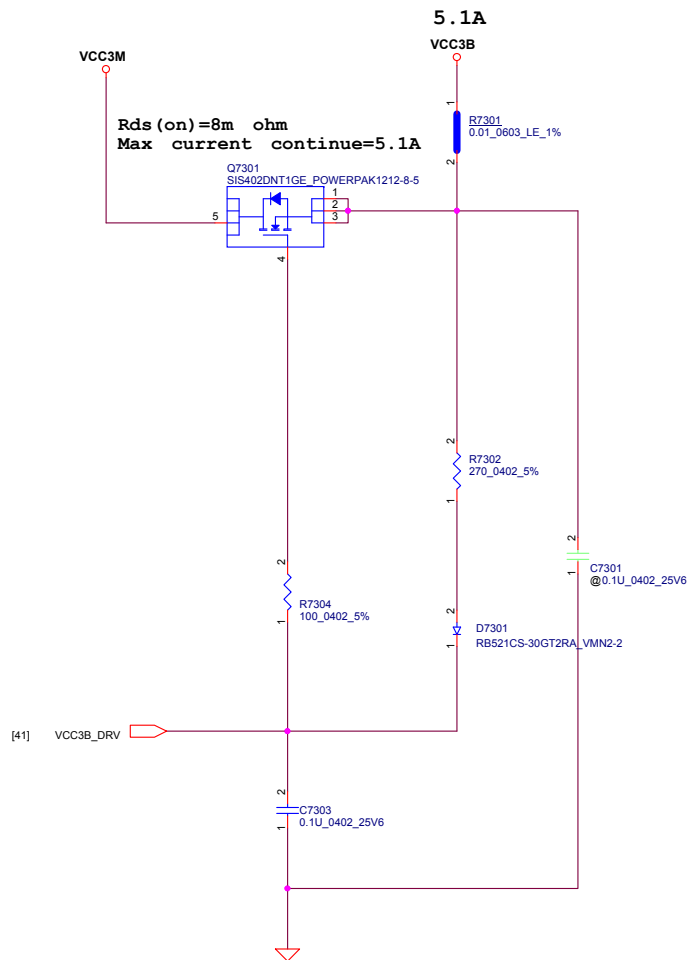
Rds (on)=65m ohm
Max current continue=4.27A

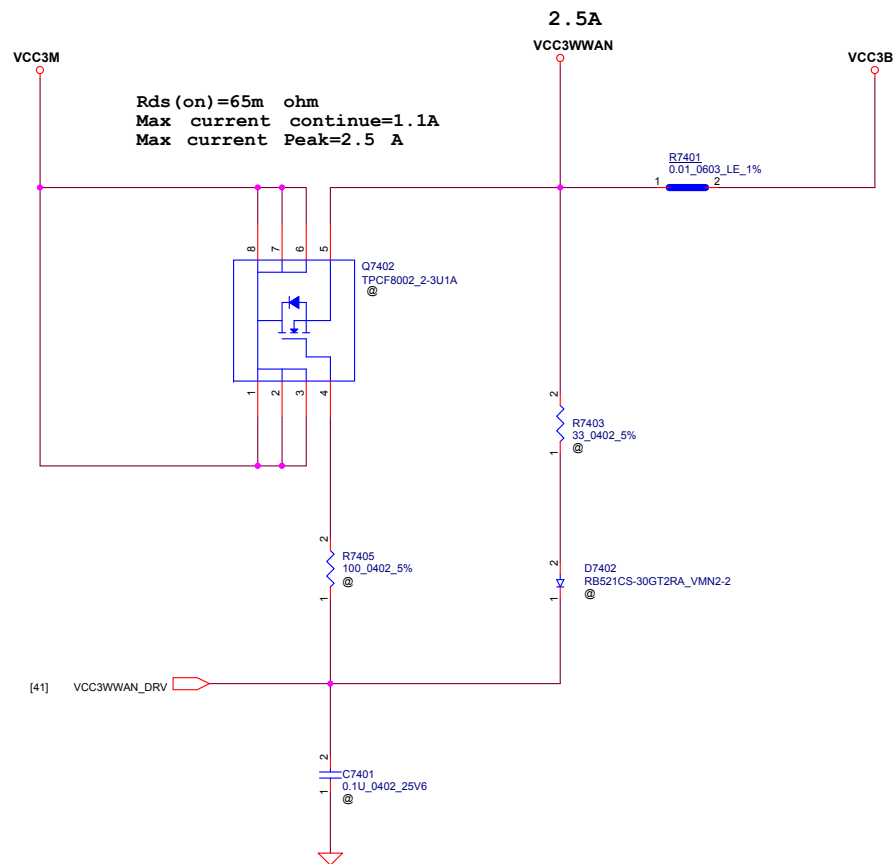
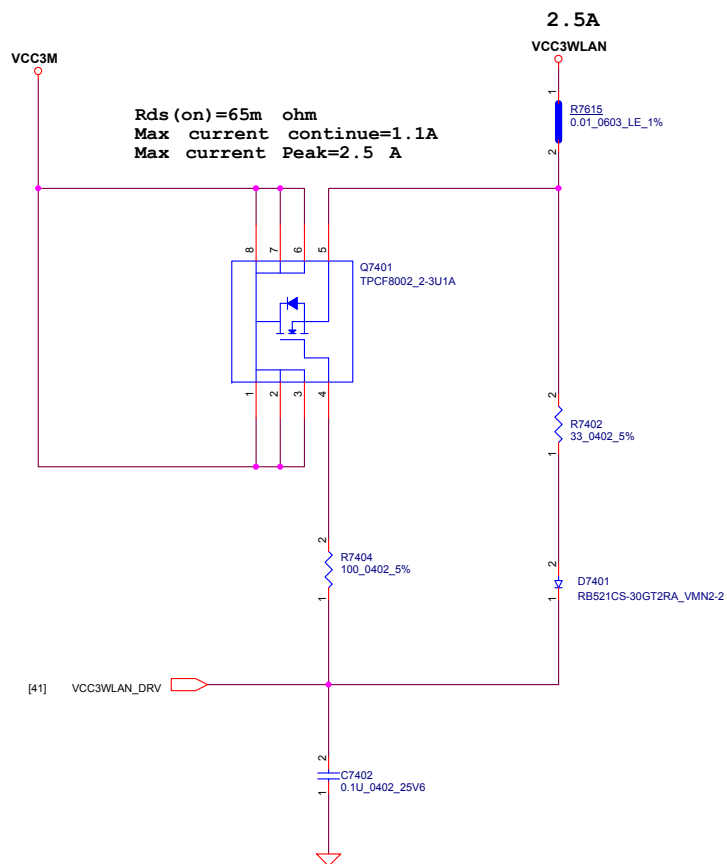



Rds (on)=371m ohm
Max current continue=15mA

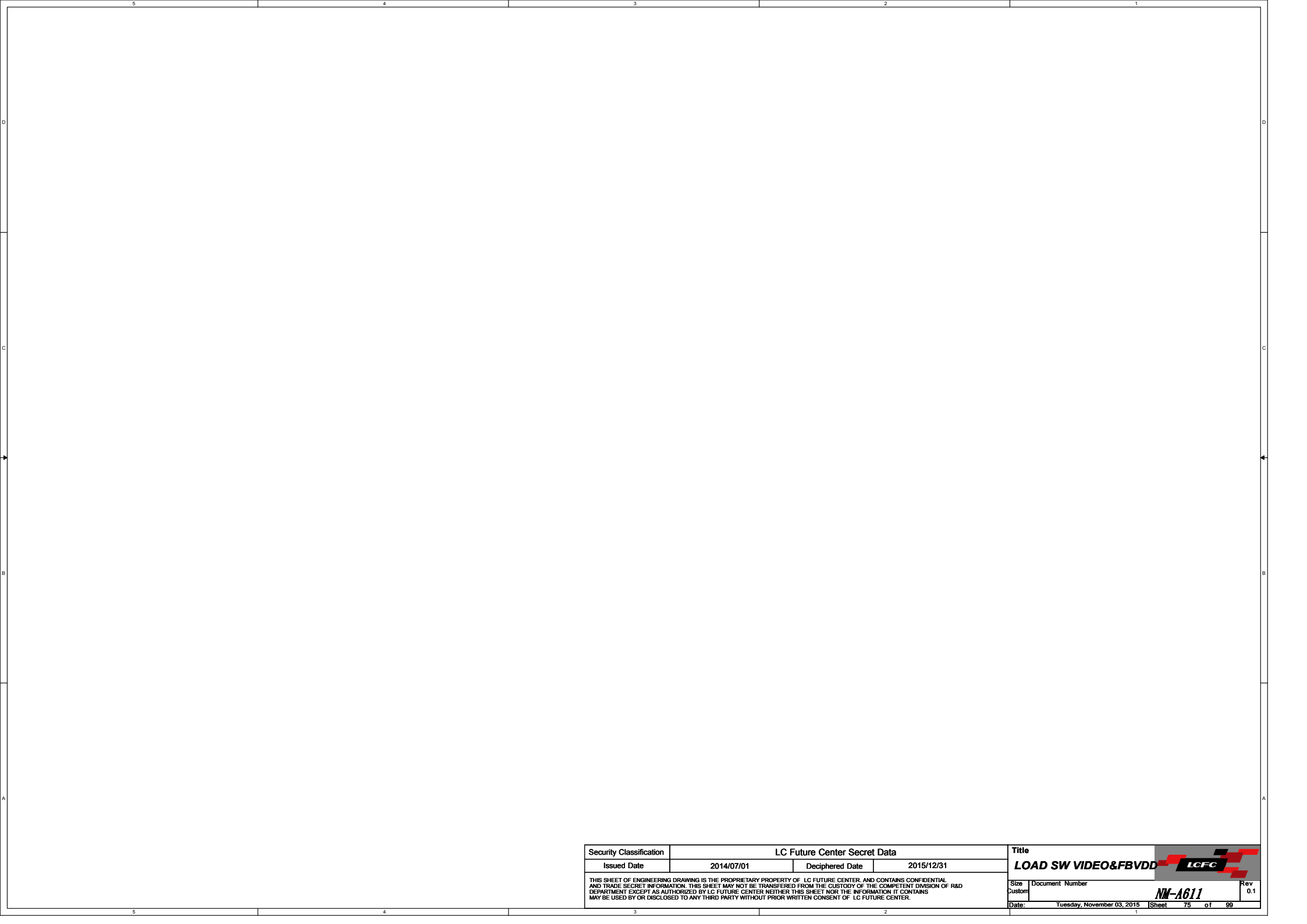


Security Classification		LC Future Center Secret Data		Title					
Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW LAN					
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				Custom		0.1			
				Date:	Tuesday, November 03, 2015	Sheet	72 of 99	NM-A611	

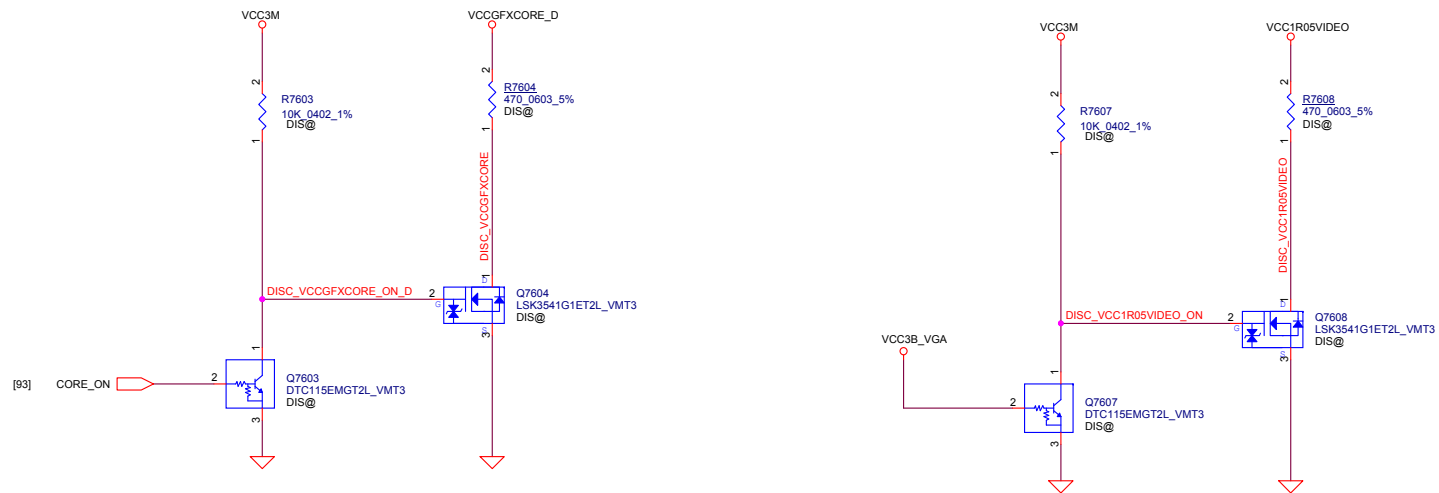




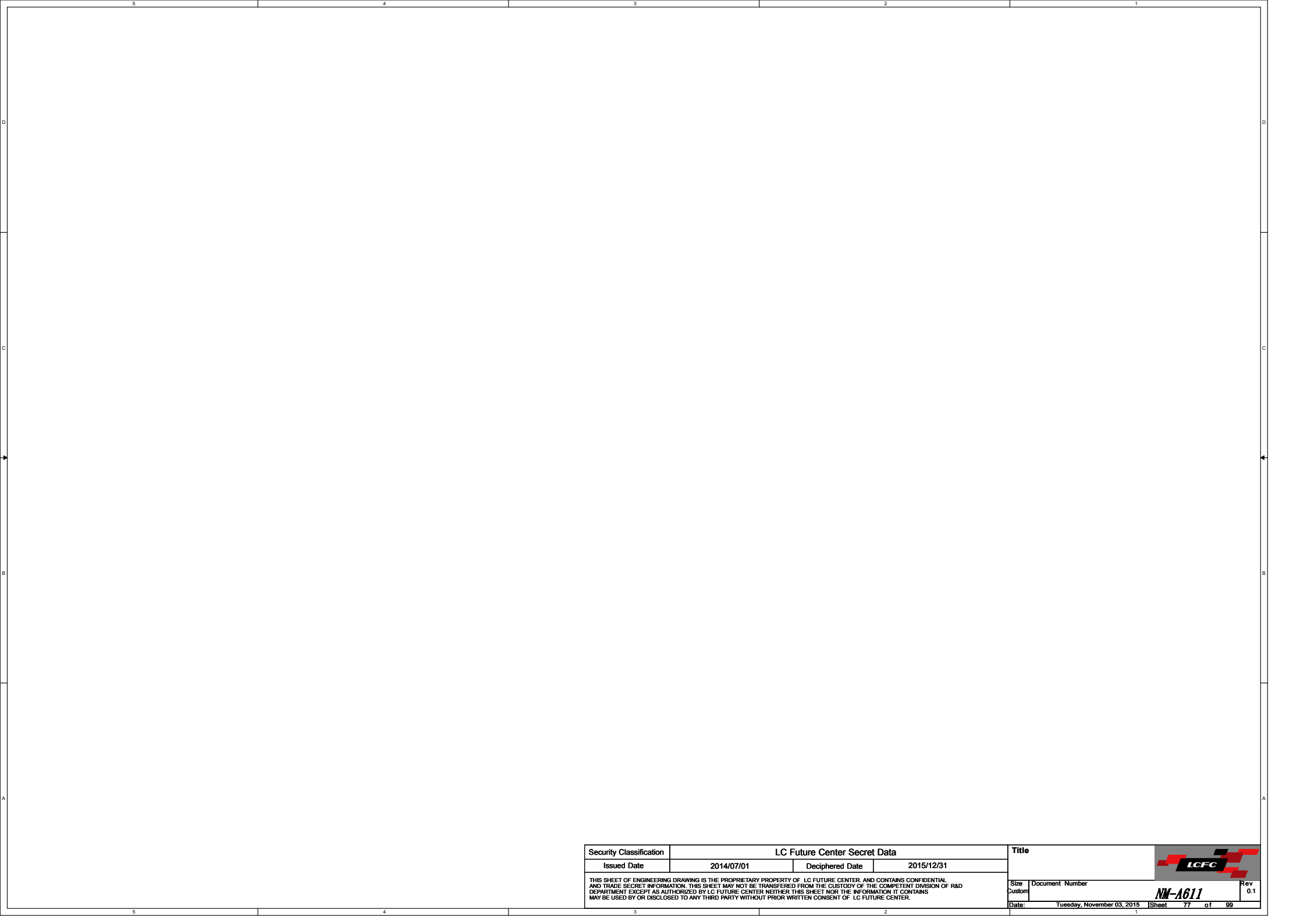
Security Classification	LC Future Center Secret Data			Title	LOAD SW WWAN&WLAN		
Issued Date	2014/07/01	Deciphered Date	2015/12/31	Size	Document Number	Rev	
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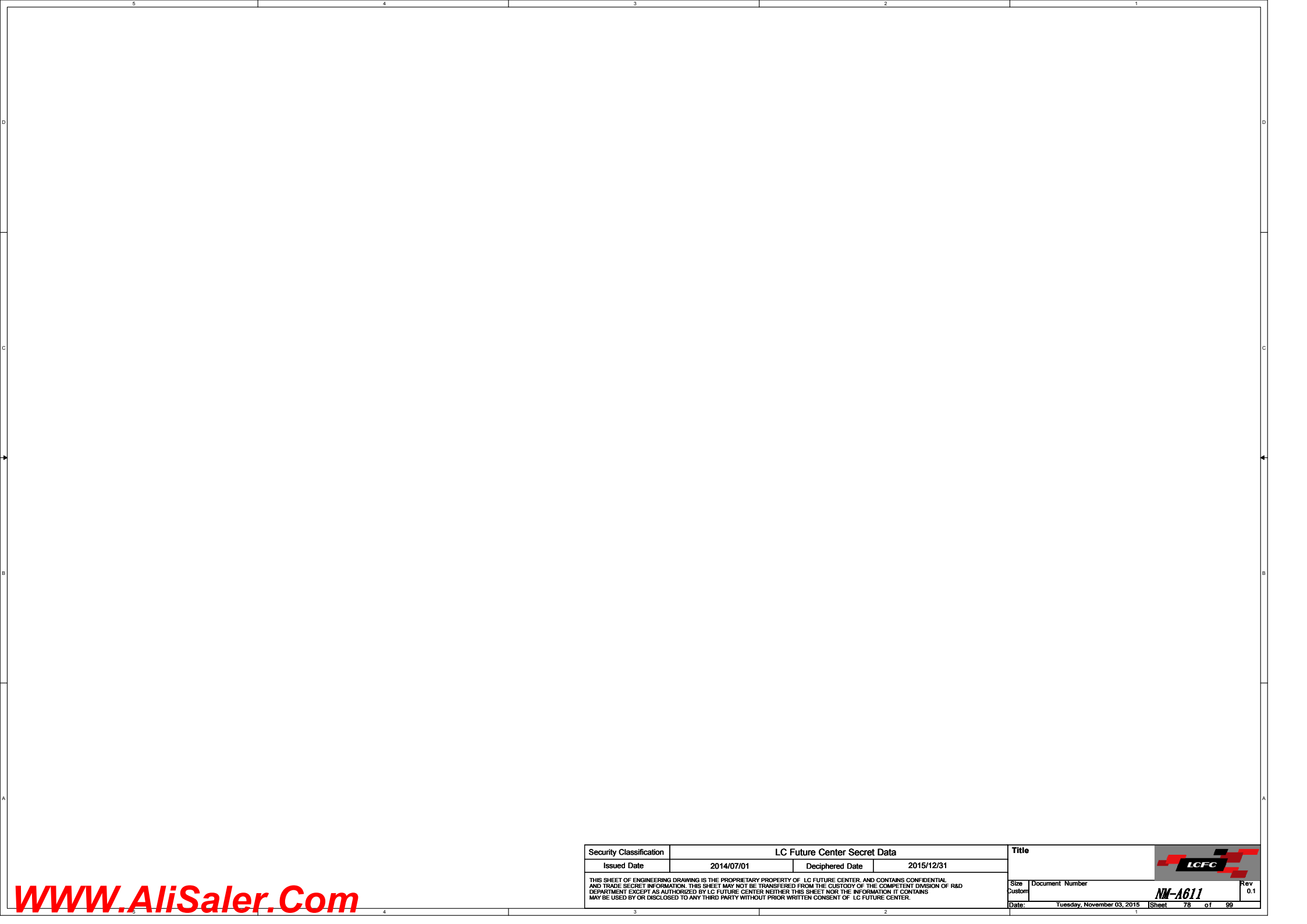
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW VIDEO&FBVDD	
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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	DISCHARGE CIRCUIT VIDEO	
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				Custom			0.1
Date:				Tuesday, November 03, 2015			
				Sheet 77 of 99			

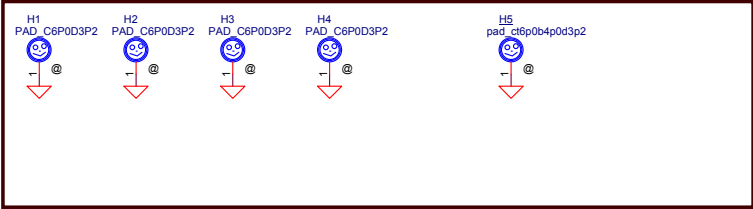


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Issued Date	2014/07/01	Deciphered Date	2015/12/31		
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				Date:	Tuesday, November 03, 2015
				Sheet	78 of 99
				Rev	0.1

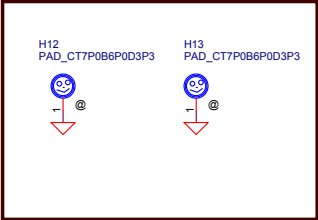


Screw Hole

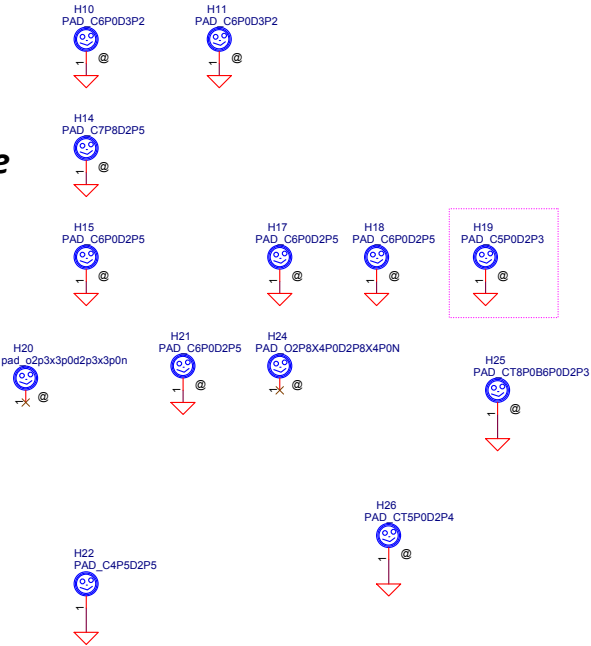
For CPU and GPU



AUDIO SCREW



For ME GND hole

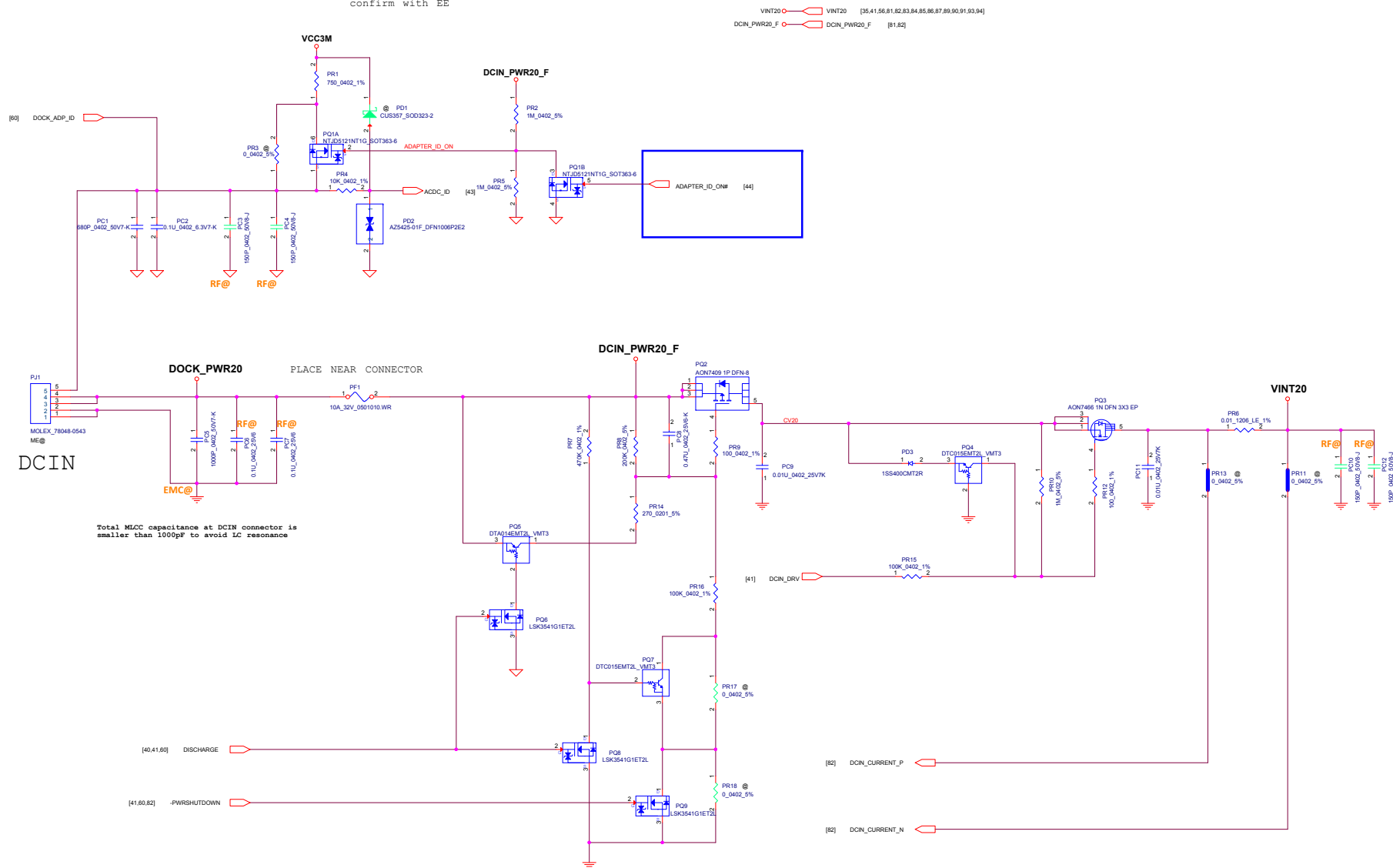


For ME hole

PCB Fedical Mark PAD



confirm with EE

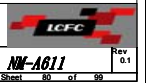


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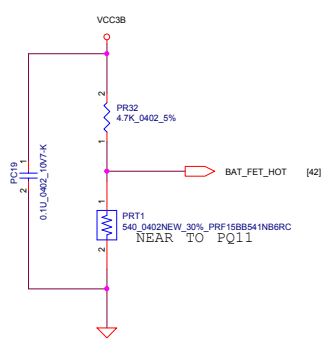
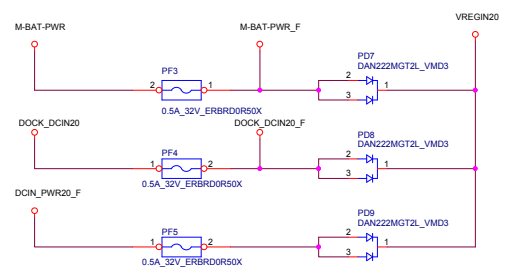
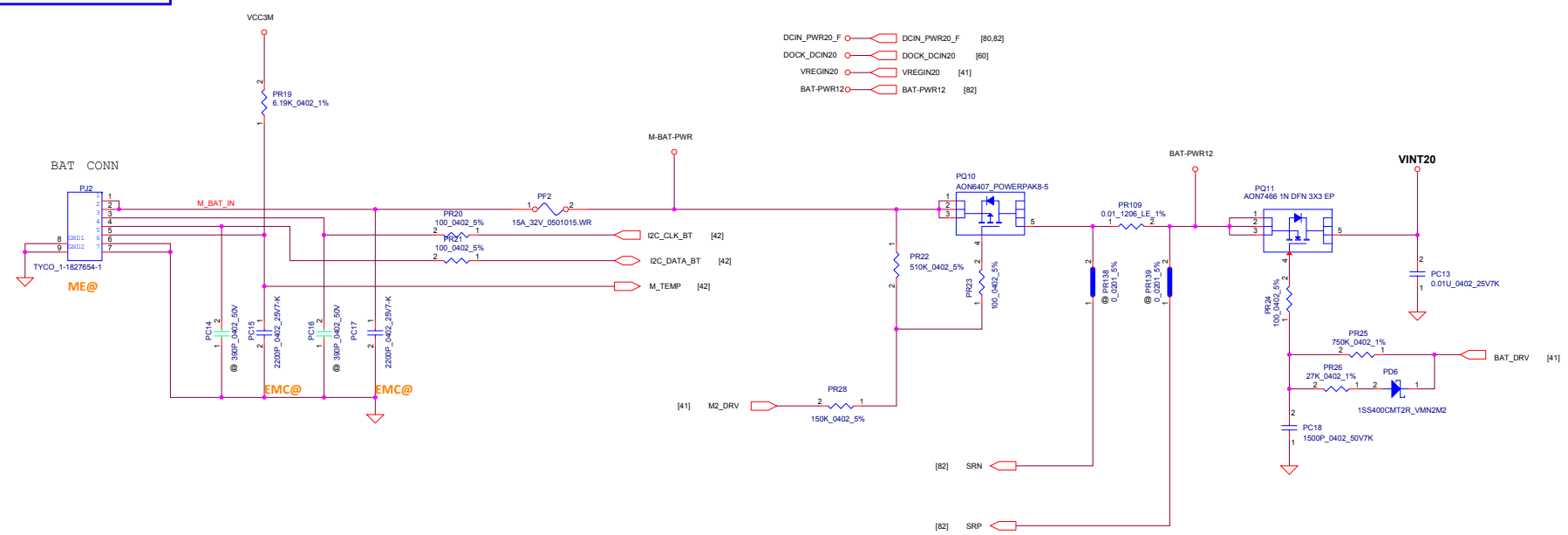
PEAK SHIFT	YES	NO
PR17	NO-ASM	ASM
PR7	ASM	NO-ASM
PQ8	ASM	NO-ASM
PQ7	ASM	NO-ASM

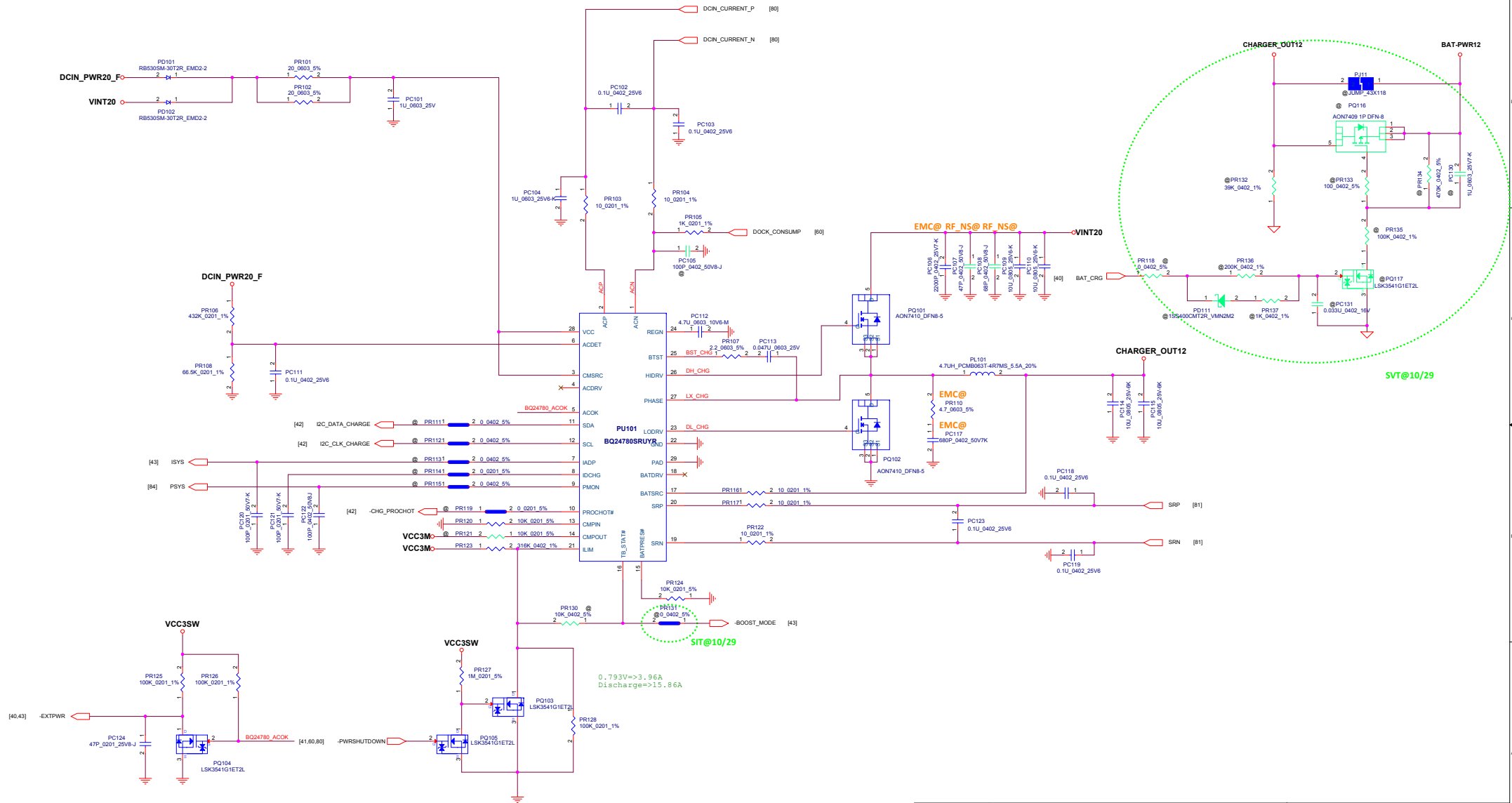
↑
LOGIC

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Payton Common



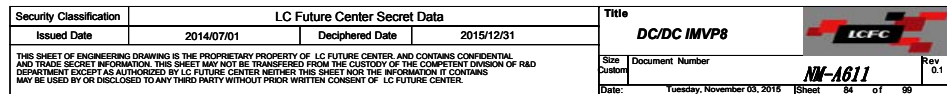


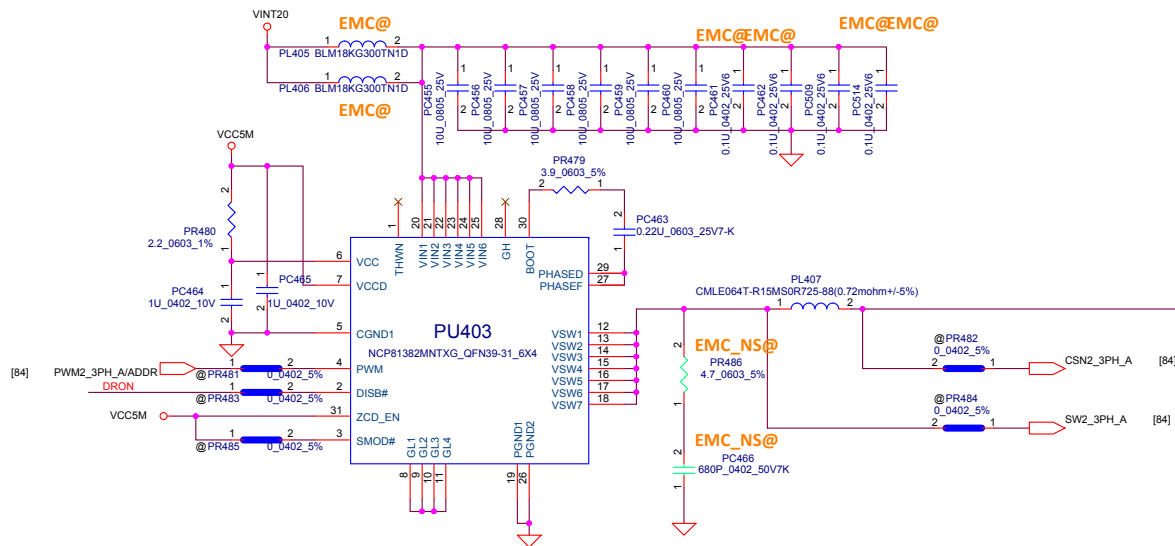
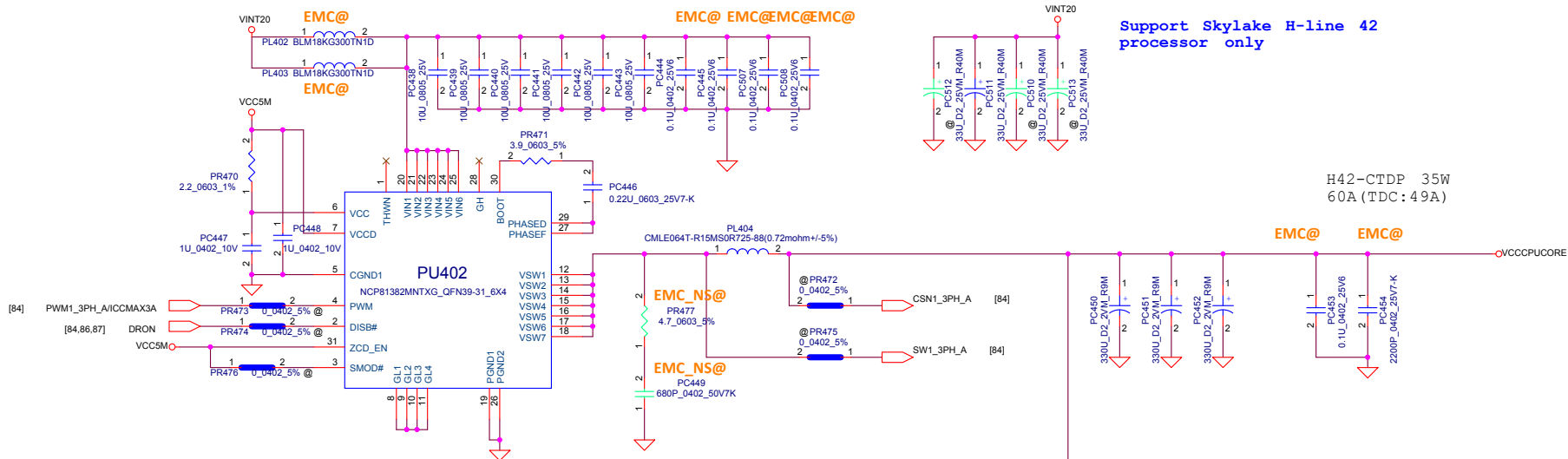
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Issued Date		Deciphered Date		BATTERY CHARGER	
Size		Document		Number	
Custom		Date		Tuesday, November 05, 2015	
		Sheet		82 of 99	





Rev 0.1
NW-4611

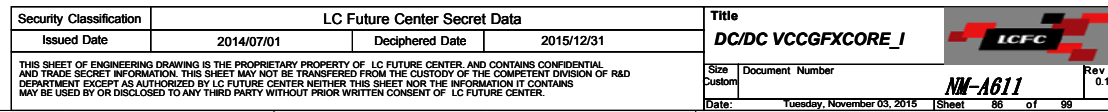
WWW.AliSaler.Com





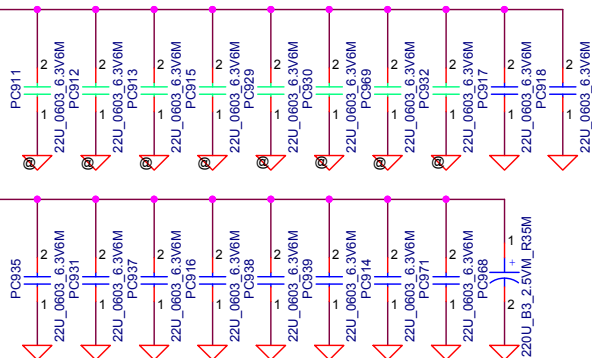
Security Classification				LC Future Center Secret Data		Title		
Issued Date		2014/07/01	Deciphered Date	2015/12/31		DC/DC VCCPUCORE		
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Support Skylake H-line 42
processor only



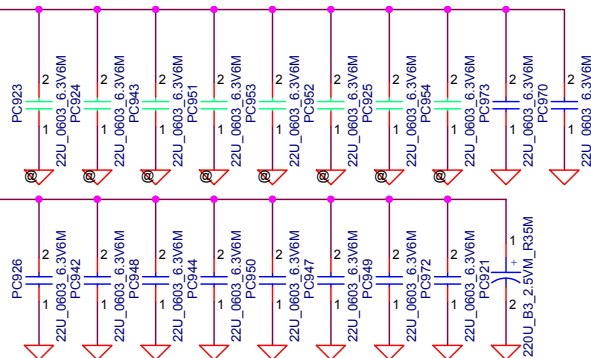
VCCCPUCORE

VCCCPUCORE
22uF 10pcs + 220uF/3528 1pcs



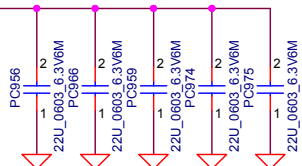
VCCGFXCORE_I

VCCGFXCORE_I
22uF 10pcs + 220uF/3528 1pcs

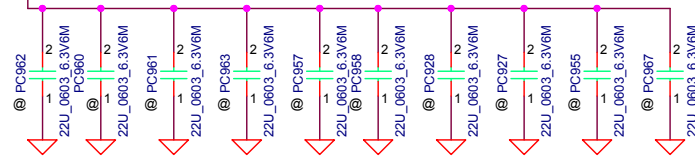


VCCSA

VCCSA
22uF 5pcs



VCCSA



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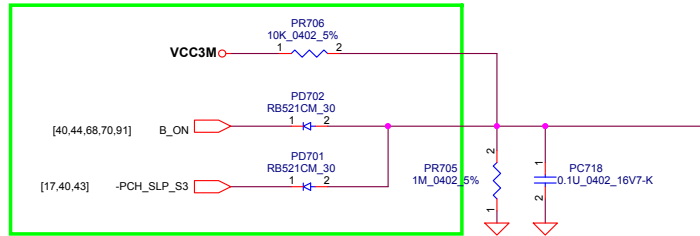
Title		Rev	
PROCESSOR DECOUPLING		0.1	
Size	Document Number	NM-A611	
Date:	Tuesday, November 03, 2015	Sheet	88 of 99



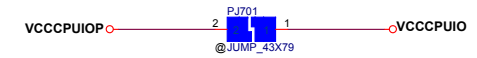
NM-A611

Rev

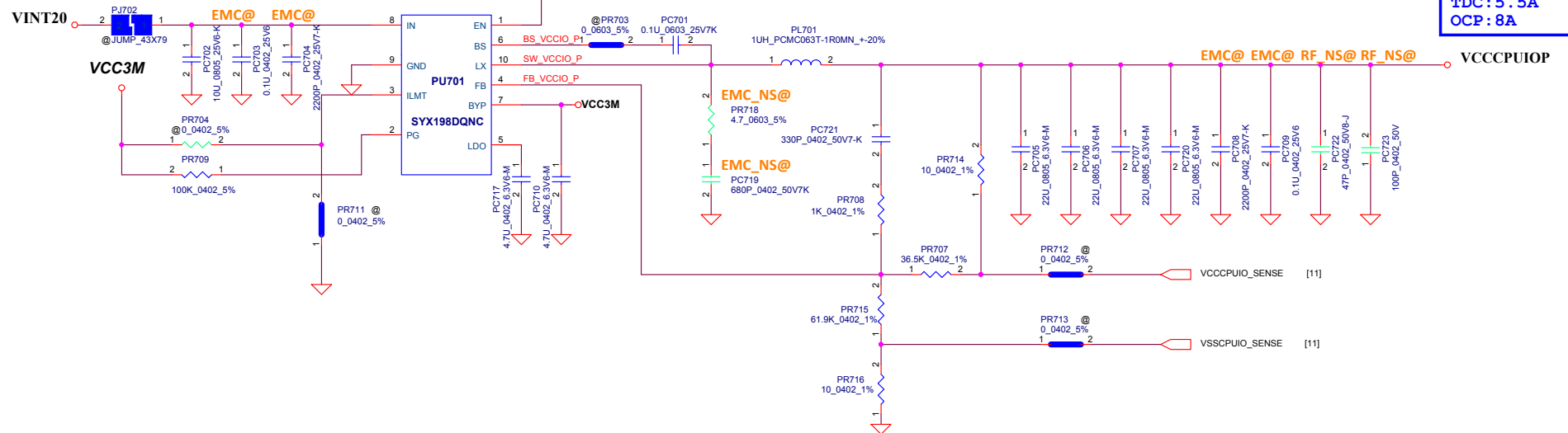
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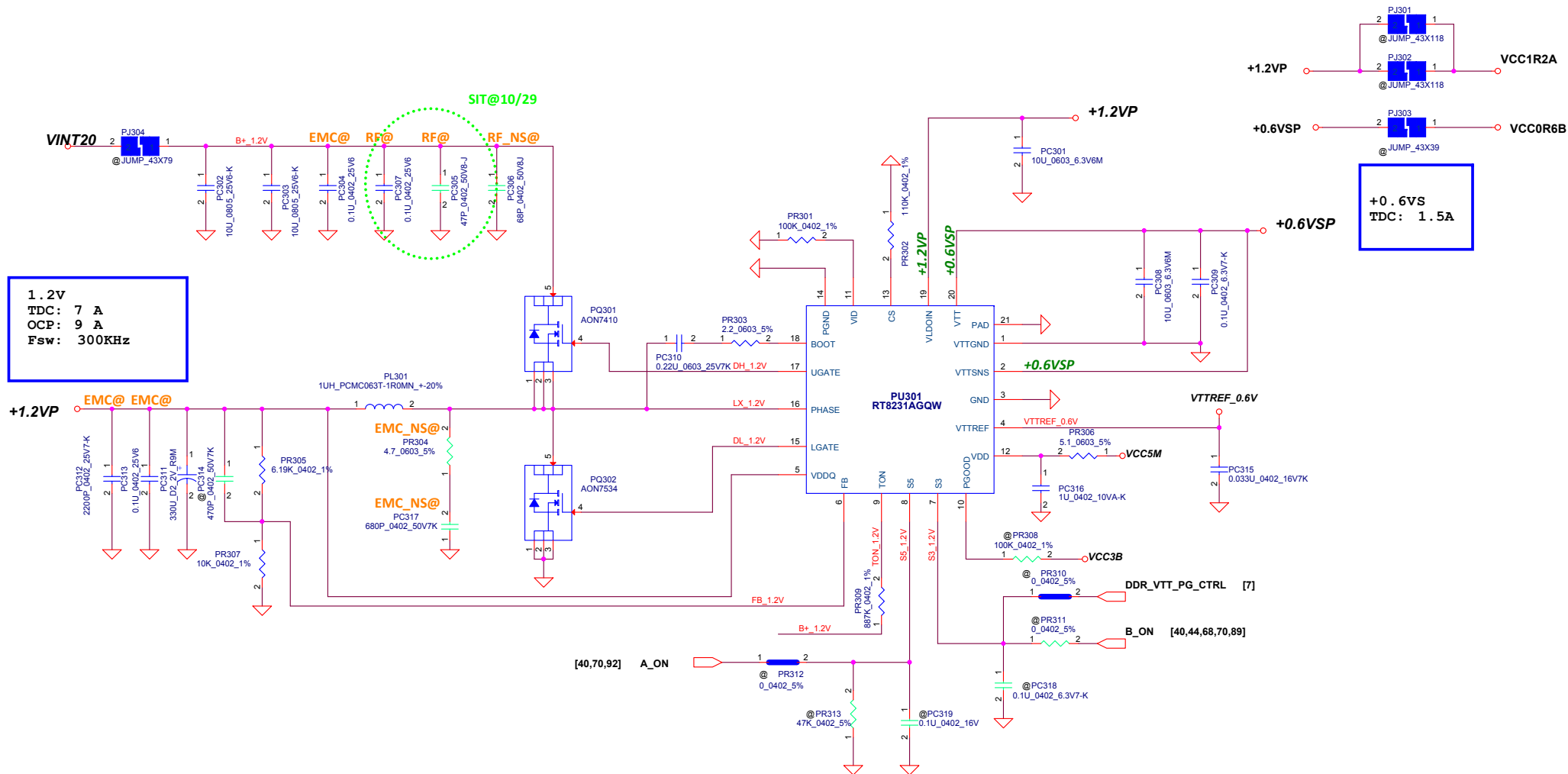


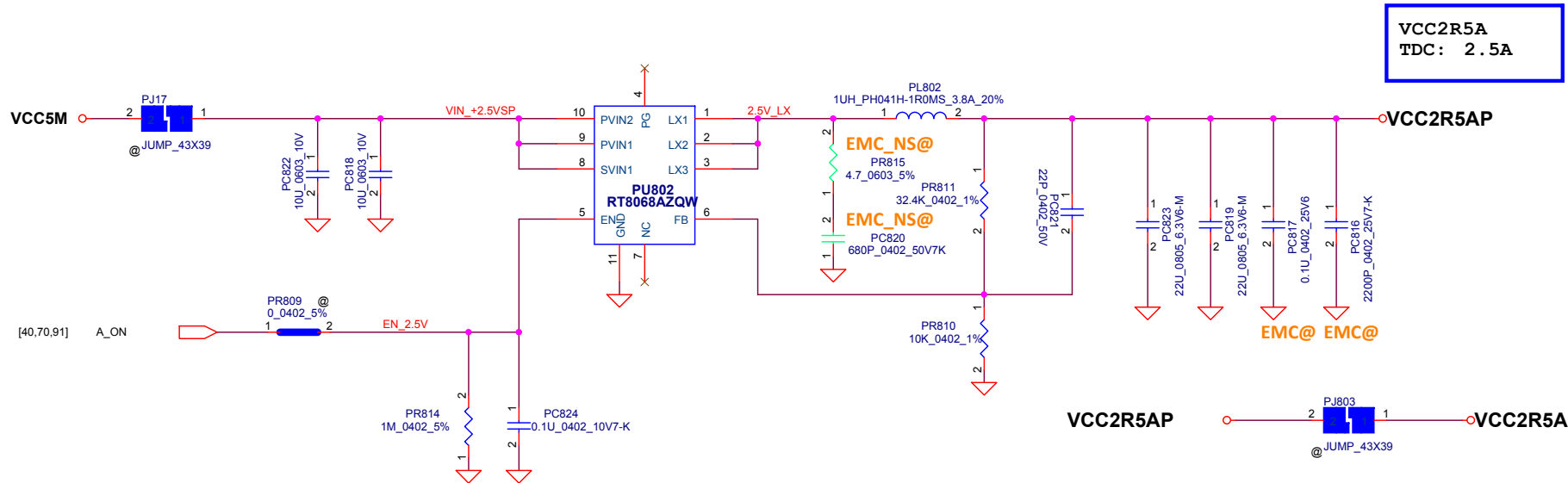
Follow Walter



VCCCPUIOP
FSW=800KHz
TDC: 5.5A
OCF: 8A



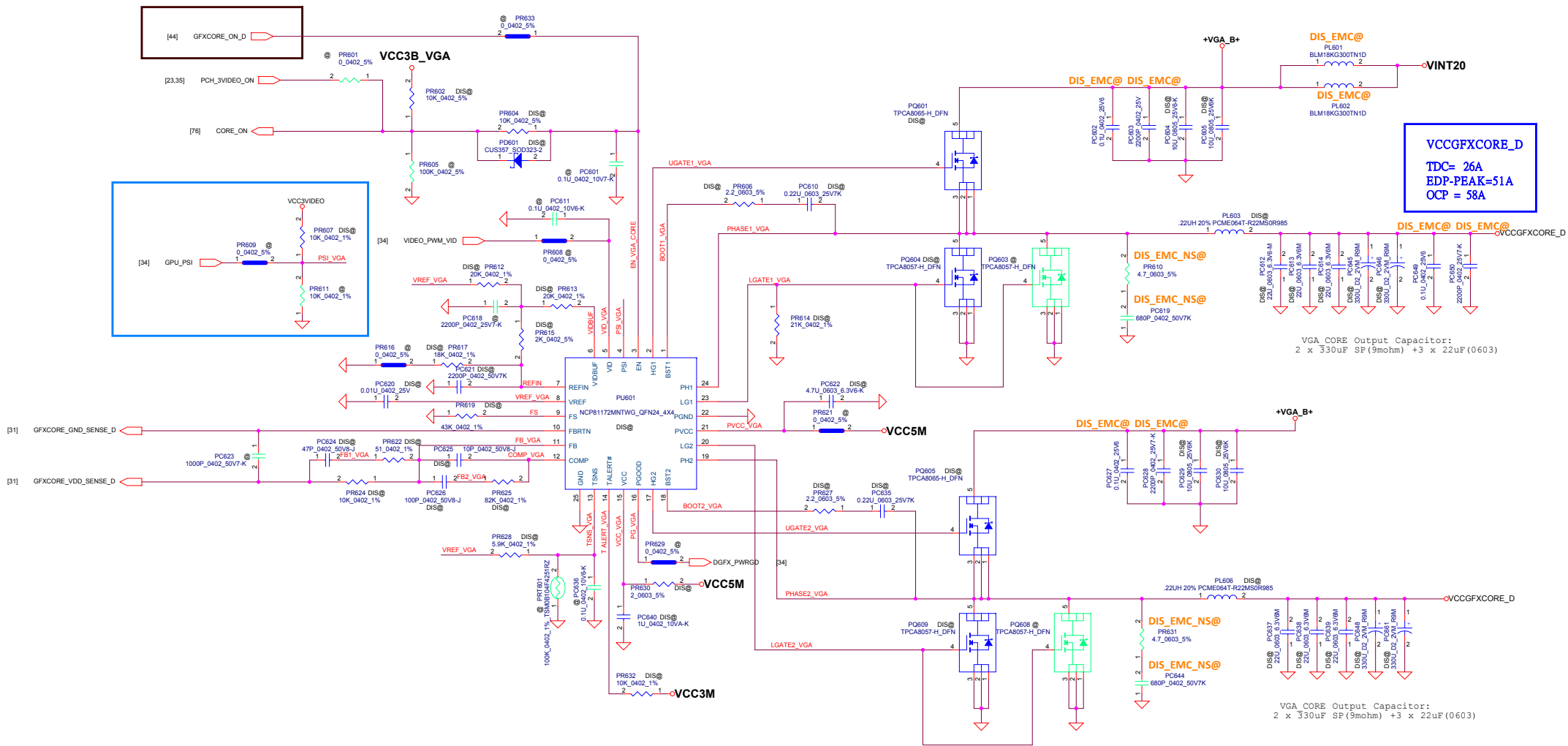




Security Classification	LC Future Center Secret Data		
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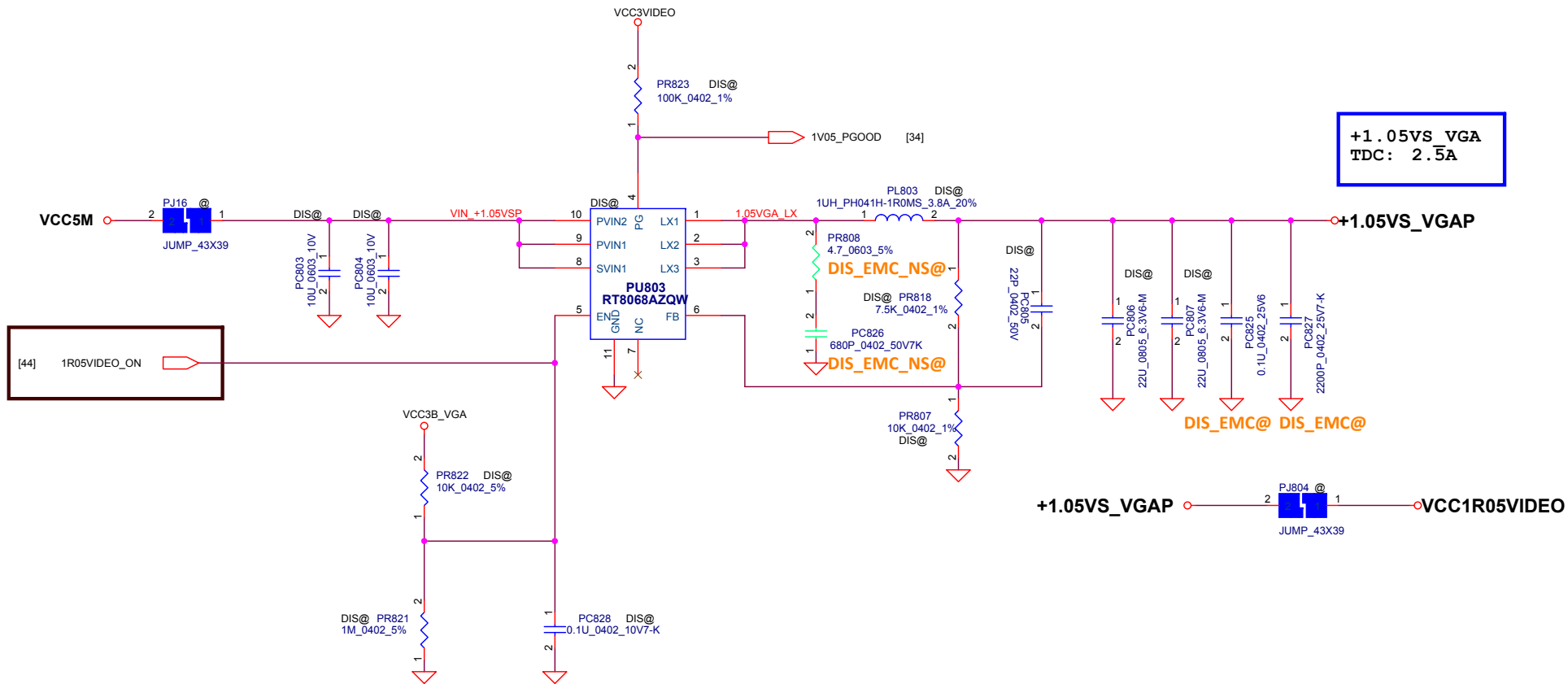
Title		DC/DC VCC2R5A	
Size	Document Number	NM-A611	
Date:	Tuesday, November 03, 2015	Sheet	92 of 99






Security Classification				LC Future Center Secret Data				Title		PWR-VGA_CORE(NCP81174)		Rev	
Issued Date		2013/08/08		Deciphered Date		2013/08/05		Size		Document Number		NM-A611	
Author								Date		Tuesday, November 03, 2015		Sheet 93 of 99	

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				3		0.1	
				Date: Tuesday, November 03, 2015			
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+0.6VSP		+0.6VSP	[91]	VINT20		VINT20	[35,41,56,80,81,82,83,84,85,86,87,89,90,91,93,94]	VCCGFXCORE_D		VCCGFXCORE_D	[31,35,76,93]	VCC3_SUS_SPI		VCC3_SUS_SPI	[19,26,55]
+1.05VS_VGAP		+1.05VS_VGAP	[95]	+3VL		+3VL	[45,47,57,67,83]	VCC3VIDEO		VCC3VIDEO	[31,34,35,93,95]	VCC5B_AVDD		VCC5B_AVDD	[45]
+1.2VP		+1.2VP	[91]	+5VL		+5VL	[40,83]	VCC3B_VGA		VCC3B_VGA	[34,35,76,93,95]	VCC5B_PVDD12		VCC5B_PVDD12	[45]
+1.5VSP		+1.5VSP	[94]	VCC3M		VCC3M	[7,14,17,21,40,41,42,43,44,51,55,56,57,62,66,68,70,71,72,73,74,76,80,81,82,83,89,93,94]	VCC1R05VIDEO		VCC1R05VIDEO	[31,33,34,76,95]	VCC3_SUS_DVDDIO		VCC3_SUS_DVDDIO	[45]
+V1.00AP		+V1.00AP	[90]	VCC3_SUS		VCC3_SUS	[7,14,15,16,17,18,21,23,24,26,42,43,45,71]	VCC1R5VIDEO		VCC1R5VIDEO	[33,34,35,37,39]	VCC3B_CPVDD		VCC3B_CPVDD	[45]
BAT-PWR12		BAT-PWR12	[81,82]	VCC3B		VCC3B	[7,16,17,18,19,20,21,23,24,27,28,35,40,41,42,43,44,45,47,49,54,55,56,57,58,59,60,61,62,67,68,73,74,81,84,90,91,94]				VCC3B_DVDD		VCC3B_DVDD	[45]	
DCIN_PWR20_F		DCIN_PWR20_F	[80,81,82]	VCC5M		VCC5M	[35,41,63,64,73,83,84,85,86,87,90,91,92,93,95]				VCC3B_DP		VCC3B_DP	[58]	
DOCK_DCIN20		DOCK_DCIN20	[60,81]	VCC5B		VCC5B	[41,45,57,59,61,65,66,67,71,73]				VCC3B_MINIDP		VCC3B_MINIDP	[59]	
DOCK_DCIN20_F		DOCK_DCIN20_F	[81]	VCCCPUCORE		VCCCPUCORE	[9,85,88]				VCC3GBE		VCC3GBE	[51,52,53]	
DOCK_PWR20		DOCK_PWR20	[60,80]	VCCGFXCORE_I		VCCGFXCORE_I	[10,86,88]				VCC3LAN		VCC3LAN	[51,72]	
M-BAT-PWR		M-BAT-PWR	[81]	VCCSA		VCCSA	[11,87,88]				VCC3M_EC		VCC3M_EC	[44]	
M-BAT-PWR_F		M-BAT-PWR_F	[81]	VCCST		VCCST	[7,11,16,24,43,70,84]				VCC3WWAN		VCC3WWAN	[62,74]	
VCC2R5AP		VCC2R5AP	[92]	VCCSTG		VCCSTG	[7,11,43,70]				VCC3WLAN		VCC3WLAN	[62,74]	
VCC3P		VCC3P	[56]	VCCCPUIO		VCCCPUIO	[5,6,11,89]				VCC5_TP		VCC5_TP	[66,71]	
VTTREF_0.6V		VTTREF_0.6V	[91]	RTCVCC		RTCVCC	[14,21,25,45]				VCC3_MC		VCC3_MC	[54]	
				VCC0R6B		VCC0R6B	[27,28,91]				VCC1R5B_AVDD		VCC1R5B_AVDD	[45]	
				VCC3SW		VCC3SW	[25,40,41,42,43,44,60,82]				+UIM_PWR		+UIM_PWR	[62]	
				VCC1R2A		VCC1R2A	[7,11,17,27,28,91]				+USB_VCCA		+USB_VCCA	[63]	
				VCC1R5B		VCC1R5B	[35,45,57,94]				LINE1_VREFO		LINE1_VREFO	[45,48]	
				VCC2R5A		VCC2R5A	[27,28,92]								
				VCC1R0_SUS		VCC1R0_SUS	[7,20,21,24,70,90]								
				VDD10		VDD10	[41]								

NOTE

1:NEED FIX SYMBOL
LV3301,LV3402,UL5201,U3401
2:NEED APPLY PART NUMBER
LV3101==>FROM BLM18PG121SN1D TO BLM15PD121SN1
3:10 OHM ALREADY CHANGE 470 OHM
RV3465,R7604,R7608